APT32F1104 Data sheet V1.3

Related documents

APT32F110X Series User Manual

Historical Version Description

Release	Modified date	Modification summary
V0.0	2020-11-13	First edition
V0.1	2021-04-13	Revise header, footer and errors in the first version, update logo
V1.1	2021-12-15	Update pinout
V1.2	2022-4	English version released
V1.3	2022-9	Update some parameters

1 Overview

1.1 Document Purpose

This document is the APT32F1104 product data sheet, including complete device usage instructions and detailed specification information.

1.2 APT32F1104 Introduction

APT32F1104 is a 32-bit, high-performance, low-cost microcontroller developed by APT Microelectronics based on the T-HEAD Semiconductor CPU core. APT32F1104 is manufactured based on embedded Flash technology, and it contains rich analog resources, including analog comparators, LCD controllers. It can be used in industrial control, small household appliances, consumer electronic equipment, wearable devices, etc.

- T-HEAD 32-bit CPU core (2-stage pipeline)
- On-chip 64K (32Kbytes optional) program flash memory, independent 2Kbytes data flash memory
- Contain 8Kbytes SRAM, which can be used for stack, data storage and code storage
- Contain 256 Bytes of non-power-down SRAM, which can be used to save CPU scene and user data when running at ultra-low power consumption
- Working temperature: 40 to 85 ^{o}C
- Operating voltage range: 1.8 to 5.5 V
- Maximum operating frequency: 48 MHz
- Interrupt Controller: Supports dynamically configured nested vector interrupts (NVIC)
- Enhanced clock and power controller (SYSCON)
- 4-Channel Direct Memory Access Controller(DMA)
- Hardware Divider (HWDIV)
- CRC Controller (CRC)
- Event Trigger Cross Bar (ETCB)
- 1x24-bit Core Timer(CORET)
- 1x Independent Watchdog Timer (IWDT)
- 1x Window Watchdog Timer (WWDT)
- 1x16-bit enhanced timer/counter (EPT), each TIMER supports 7 PWM output functions and complementary dead zone mode(EPT0)
- 1x 24-bit 2 channels general-purpose timer/counter, supporting PWM functions (GPTA0)

- 1x 16-bit 2 channels general-purpose timer/counter, supporting PWM functions (GPTA1)
- 2x 16-bit 3 channels general-purpose timer/counter, supporting PWM functions and complementary dead zone mode (GPTB0~ GPTB1)
- 1x 16-bit counter (COUNTERA), support auto-reload function and single or cycle counting function (carrier generator)
- 2x 16-bit basic timer (Basic Timer)
- 1x 16-bit low-power TIMER (LPT)
- 1x 16-bit RTC
- Serial communication interface: 1x I2C, 3x UART, 1x USART,1 x SPI, 1 x SIO
- Up to 19 channels of 12-bit ADC, supporting external AVREF input
- 10x High-current-driven pins (each pin supports a maximum current of 120mA)
- Support 8 COM x 26 SEG or 4 COM x 30 SEG LCD driver, Cap-bias and R-bias modes are optional
- Support 2 independent analog comparators
- Support internal reference voltage source of 1.0 V and internal fixed voltage source of 2.048 V/4.096 V
- Support 96 bit UID
- Support up to 44 PIO, all GPIO can be configured as external interrupts
- Support RUN, SLEEP, SNOOZE，DEEP-SLEEP and SHUTDOWN mode

1.3 Main Features

1.3.1 Processor (CPU）

- 32-bit RISC CPU core, 16-bit instruction length
- 16x 32-bit general registers
- Efficient 2-level execution pipeline
- Single-cycle 32-bit x 32-bit hardware shaped multiplication array
- SWD (Serial Wire Debug) debug interface

1.3.2 Memory

- Up to 64Kbytes of internal program flash memory, support ISP protection, the size of the protection area can be configured, support CRC check
- Up to 2Kbytes of independent data flash memory, the program operation will not be interrupted when the data flash is updated
- User Option configuration
    - External reset pin enable configuration
    - Watchdog default enabled state configuration
    - Code security configuration
- Dedicated programming interface, supporting rapid mass production programming (need to cooperate with a dedicated programming device)
- Up to 8Kbytes of internal SRAM with parity check support
- Up to 256 bytes SRAM without power down, support parity check
- Little-endian storage method

1.3.3 Nested Vector Interrupt Controller（NVIC）

- Up to 32 interrupt sources
- 32 programmable priority levels, each interrupt has an independent priority level
- Each interrupt has independent enable or disable control
- Each interrupt source has a fixed vector address
- Support trap function
- Support software reset
- Global interrupt enable control
- Individually configurable enable/disable for wake-up events and interrupts

1.3.4 System Controller(SYSCON)

- External crystal oscillator 32.768KHz to 24MHz (EMCLK: External Main Clock)
- External auxiliary oscillator 32.768KHz (ESCLK: External Sub Clock)

- Internal main oscillator 131.072KHz / 2.097MHz / 4.194MHz / 5.556MHz (default) four option selections (1% deviation @typical value, IMCLK: Internal Main Clock, internal main clock)
- Internal high-speed oscillator 48MHz (1% deviation @typical value, HFCLK: High Frequency Clock, internal high-speed clock)
- Internal auxiliary oscillator 27KHz (5% deviation @typical value, ISCLK: Internal Sub Clock, internal auxiliary clock)
- All internal oscillators support software fine-tuning
- Support low power consumption mode (SLEEP/ SNOOZE/DEEP-SLEEP)
- Support programmable power optimization in low power mode
- Programmable clock divider
- External crystal oscillator failure monitoring (when the external crystal oscillator fails, it supports automatic switching to the internal main oscillator)
- External crystal jitter filter processing
- External interrupt input digital filter control, support asynchronous counting triggered by interrupt
- FLASH and SRAM check error management, configurable retry or system reset
- Reset source detection and management (RSTID)

1.3.5 Direct Memory Access（DMA）

- Support up to 4 channels
- Flexible and configurable read and destination addresses
- Trigger source controlled by ETCB and support all internal trigger events

1.3.6 Hardware Divider（HWDIV）

- Signed or unsigned 32-bit integer division
- Support 32-bit dividend and 32-bit divisor, output 32-bit quotient and remainder
- 5 HCLK cycle operation time
- Support divide-by-zero overflow error interrupt

1.3.7 Independent Watchdog Timer（IWDT）

- Configurable reset time: 8 seconds by default
- Configurable alarm interrupt before reset
- Programmable 18-bit down counter (27KHz clock) independently work under the internal auxiliary crystal oscillator

1.3.8 Window Watchdog Timer（WWDT）

- Work based on PCLK
- Support alarm interrupt before reset
- Software-triggered reset operation

- Counter refresh window to limit function

1.3.9 16-bit Enhance Purpose Timer/Counter（EPT）

- Three counting modes: increment, decrement, increment and decrement
- Each TIMER has 4 independent PWM outputs, supports 4 comparison values and up to 7 PWM outputs
- Support complementary output, dead zone control, chopping output, emergency mode output
- Support emergency mode output: soft lock and hard lock mode
    - External input EPIx
    - System error, LVD interrupt triggered
- Support special register protection
- Support single trigger mode and external pulse counting mode
- 4x digital comparators can trigger a variety of synchronization and waveform output
- Support working in capture mode and up to 4 capture of comparison values
- Support ETCB event linkage
- PCLK working clock

1.3.10 16-bit General Purpose Timer/Counter A（GPTA）

- Three counting modes: increment, decrement, increment and decrement
- Each TIMER supports two output channels, and each channel can be configured as PWM waveform output control
- Support capture mode, up to 4 capture values
- Support ETCB event linkage
- PCLK working clock

1.3.11 16-bit General Purpose Timer/Counter B（GPTB）

- Three counting modes: increment, decrement, increment and decrement
- Each TIMER supports three output channels, and each channel can be configured as PWM waveform output control
- Support complementary output, dead zone control, chopping output, emergency mode output
- Support capture mode, up to 4 capture values
- Support ETCB event linkage
- PCLK working clock

1.3.12 Counter A (CNTA)

- 1x 16-bit counter, support automatic reload function and single or cycle counting function
- Software/hardware selectable carrier frequency output enable/disable control
- Within a periodic waveform, the output high/low pulse width is configurable

- Configurable output polarity
- Drive speakers or remote IR data transmission

1.3.13 Basic Timer (BT)

- 1x 16-bit up counter, supporting automatic reload function
- Support PWM waveform output
- Counting clock supports independent prescaler configuration
- Support compare interrupt, period interrupt and overflow interrupt

1.3.14 Core Timer (CORET)

- 1x 24-bit down counter, supporting automatic reload function
- Counting clock source is optional (CPU clock or system clock divided by 8)
- Support periodic interrupt and overflow interrupt

1.3.15 Low Power Timer (LPT)

- 16-bit up counter, support auto reload function
- A 16-bit comparison value register, supporting PWM output
- 3-bit prescaler selection, support 1, 2, 4, 8, 16, 32, 64, 128 frequency division
- Support multiple counting clock sources: ISCLK, IMCLK, EMCLK, PCLK or external CLK
- Support Toggle or PWM output function
- Support single trigger mode
- Support periodic interrupt and MATCH interrupt
- Support ETCB event linkage

1.3.16 Real Time Counter（RTC）

- Only POR reset is valid, support write protection
- Timing function: support hour (12 or 24 hour format), minutes, seconds and sub-seconds, BCD format
- Calendar function: support year, month, day and week, BCD format, automatic leap year recognition
- Support optional clock sources: external crystal oscillator (support 32.768KHz), internal main oscillator IMCLK and internal secondary oscillator ISCLK
- Support 2 programmable alarm clocks
- Support periodic wake-up
- Digital calibration function
- Support ETCB event linkage
- Programmable frequency output (output through CLO)

1.3.17 Universal Asynchronous Receiver Transmitter（UART）

- 3 channels
- 8-bit data length, support parity bit (parity check, 0/1 check)
- Separate 8x8 bit transceiver FIFO
- Programmable baud rate

1.3.18 Universal Synchronous/ Asynchronous Receiver Transmitter（USART）

- 1 channel
- Support 5, 6, 7 and 8 bit data length
- Separate 8x8 bit transceiver FIFO
- Programmable baud rate
- Check Digits, Frame Detection and Buffer Overflow Error Reporting
- Support Loop-back mode
- Support synchronous full-duplex mode
- Support LIN bus protocol: LIN1.2 or LIN2.0
- Support Smart Card Protocol: ISO7816-3 Compliant

1.3.19 Inter-Integrated Circuit（I2C）

- 1 channel
- Support multi-master I2C bus, support master or slave working mode.
- Standard mode 100Kbit/s, high-speed mode up to 400Kbit/s, ultra-high-speed mode up to 1Mbit/s
- Compatible with serial 8-bit data transmission and two-way data transmission
- 7-bit or 10-bit addressing
- Automatic bus recovery function
- Separate 8x8 bit transceiver FIFO

1.3.20 Serial Peripheral Interface（SPI）

- 1 channel
- Programmable data frame length: 4 to 16 bits
- Support host and slave mode
- Separate 8x16-bit transceiver FIFO

1.3.21 Serial Input and Output Interface（SIO）

- single-wire communication pin, two-way data transmission
- Various communication rates can be obtained by configuring clock frequency division
- Receive mode requires synchronization to start flag

- In receive mode, the number of samples and decimation points per bit (bit) can be adjusted
- In receive mode, input filtering can be flexibly configured

1.3.22 AD Converter

- Up to 19 analog input channels for selection, the reference voltage supports VDD or external pins
- ADC input supports external ADCIN or 1/4VDD and internal high-precision voltage reference source (INTVREF)
- Support the fastest 1MSPS conversion speed
- Support continuous conversion mode and conversion results of hardware comparison
- Support multi-sequence conversion mode, up to 16 conversion sequences, flexible configuration of conversion channels, conversion order, conversion times
- Support continuous sampling or single sampling, flexibly configurable sampling priority
- Support ETCB event linkage

1.3.23 Internal Voltage Reference（INTVREF）

- As ADC sampling channel calibration input
- As VREF input of ADC (ADC must work in low speed state)
- Reference voltage: 1.0V (The actual measured value of the factory can be read through the register)

1.3.24 Fixed Voltage Reference（FVR）

- As VREF input of ADC
- Reference voltage: 2.048V/4.096V

1.3.25 Comparator（COMP）

- Support 2 independent analog comparators
- Configurable comparator output hysteresis and digital debounce filtering
- Support comparator output via specific event window capture function

1.3.26 Liquid Crystal Display Controller（LCDC）

- Support 30x4 or 26x8 mode LCD driver
- Support Cap-bias and R-bias mode optional
- Support grayscale adjustment
- Support Blinking mode
- Support 1/2、1/3、1/4 and 1/8 duty
- Support 1/2、1/3 and 1/4 bias
- LCD display RAM supporting double buffering

1.3.27 Cyclic Redundancy Check（CRC）

- Support writing operations based on Byte, Half-word, Word
- The selectable CRC polynomials include:
  - CRC-CCITT：$X^{16} + X^{12} + X^5 + 1$
  - CRC-16：$X^{16} + X^{15} + X^2 + 1$
  - CRC-32：$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^3 + X^2 + X + 1$
- Programmable seed value
- Programmable endianness setting (LSB first or MSB first), selection of input data and CRC checksum are operated in complement form

1.3.28 Event Trigger Cross Bar（ETCB）

- Support configurable interconnect triggering between on-chip modules
- Support up to 12 trigger channels
- Each channel supports 64 Source input options
- Each channel supports 64 Target output options
- Each channel supports software trigger

1.3.29 General-Purpose IO (GPIO)

- 48 pins: up to 44 GPIO
- Push-pull output and open-drain output are configurable, pull-up and pull-down resistors are configurable
- Support output status monitoring, each IO drive capability can be configured independently (10 IO support high current sink)
- All pins support external interrupt function and up to 20 external interrupts at the same time

1.3.30 Two Low-power Modes

- SLEEP: Turn off the selected system clock and CPU clock
- DEEP-SLEEP: Turn off all system clocks and CPU clocks and hold the logic state
- SNOOZE：The CPU logic is powered off, keeping the RAM data, the TKEY/LCD/I2C module can choose whether to power off or not, and the PAD function is normal. Configurable wake-up source: external interrupt, iWDT interrupt, LVD interrupt, RTC interrupt or LPT interrupt
- SHUTDOWN: RAM data is not saved, a small part of the logic state is maintained, most of the logic is powered off, most of the PADs remain in the state before SHUTDOWN, and a small part of the PADs maintain normal functions. Configurable wake-up source: WKI, iWDT interrupt, LVD interrupt, RTC interrupt or external reset

1.3.31 Power On Reset（POR）

- Reset voltage: 1.45V

1.3.32 Low Voltage Detector（LVD）

- Configurable low voltage reset function, optional 8 voltage values (1.9V/2.2V/2.5V/2.8V/3.1/3.4/3.7/4.0)
- Configurable low voltage interrupt, optional 8 voltage values (2.1V/2.4V/2.7V/3.0V/3.3/3.6/3.9/LVDIN)

1.3.33 Operating Voltage Range

- 1.8V to 5.5V

1.3.34 Operating Frequency Range

- External main crystal oscillator: 32KHz ~ 24 MHz
- Internal oscillator: IMOSC: 5.557 MHz (max) / HFOSC: 48 MHz (max)
- Internal auxiliary vibration: 27KHz

1.3.35 Operating Temperature Range

- – 40 to 85°C

1.3.36 Package

- 48-LQFP
- 44-QFP
- 32-LQFP
- 32-QFN

1.4 Resource Summary

Table 1-1 APT32F1104 Resource Feature Comparison

ITEM	APT32F1104		
	48 Pin Package	44Pin Package	32 Pin Package
FLASH (Kbytes)	64	64	64
SRAM (Kbytes)	8	8	8
EPT	1	1	1
16-bit GPTA	2	2	2
16-bit GPTB	2	2	2
16-bit LPT	1	1	1
16-bit BT	2	2	2
RTC	1	1	1
UART	3	3	2
USART	1	1	1
SPI	1	1	1
I^2C	1	1	1
SIO	1	1	1
IWDT	1	1	1
WWDT	1	1	1
ADC input channel	19	17	12
LCD	8 com x 26seg	8 com x 24seg	8 com x 15seg
CMP input channel	8	6	3
GPIOs (HS)(1)	44(10)	41(10)	29(6)
CPU frequency	48MHz	48MHz	48MHz
Operating Voltage	1.8V ~ 5.5V	1.8V ~ 5.5V	1.8V ~ 5.5V

NOTE: (1) HS means High Sink Current IO

1.5 Block Diagram

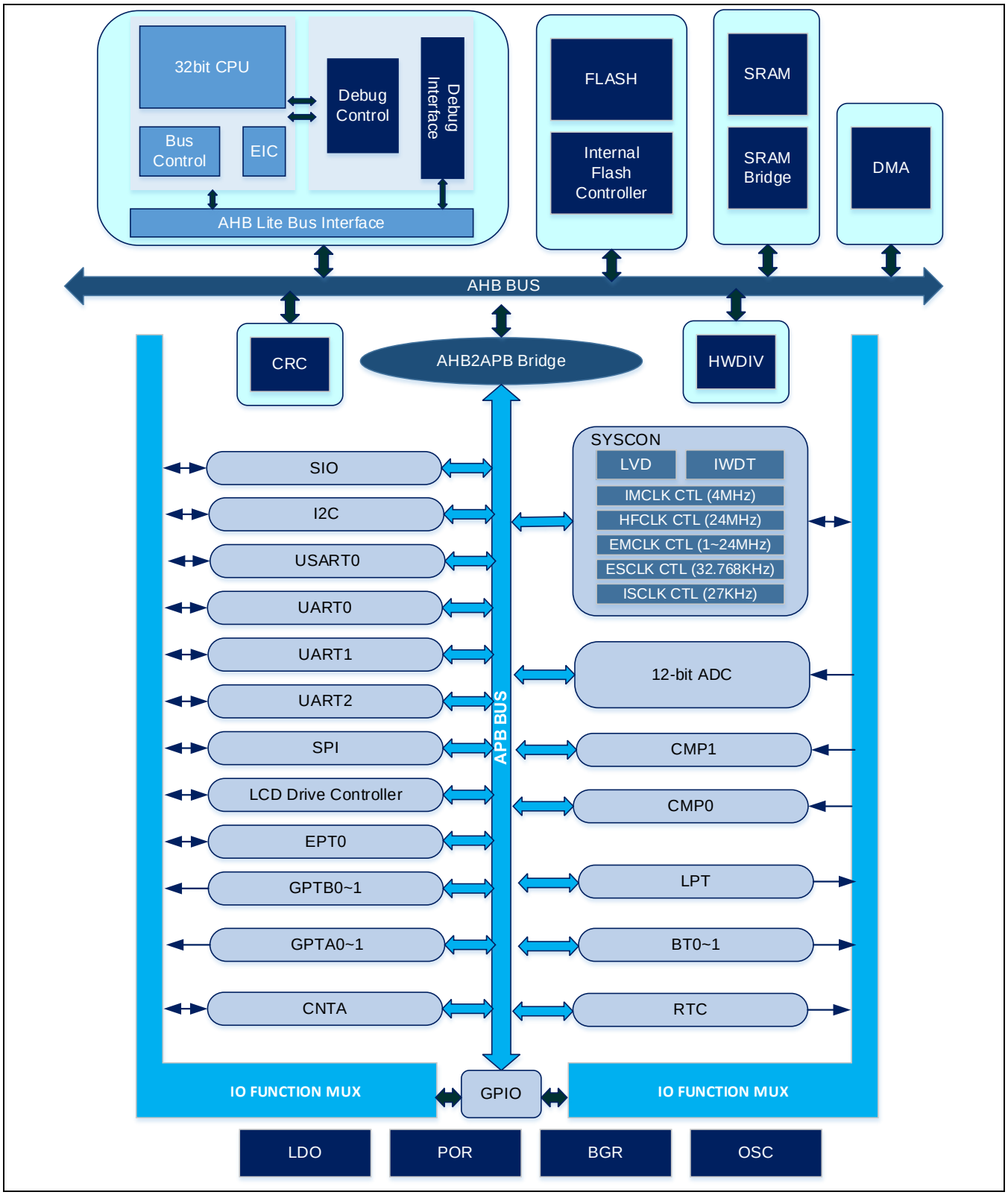


Figure 1-1 APT32F1104 Block diagram

2 Pin Configuration

2.1 Summary

This chapter describes the pin function information of the APT32F1104 product.

contain:

- Pin map
- Pin allocation table
- Remap pin
- Pin description

2.2 Pin Definition Diagram

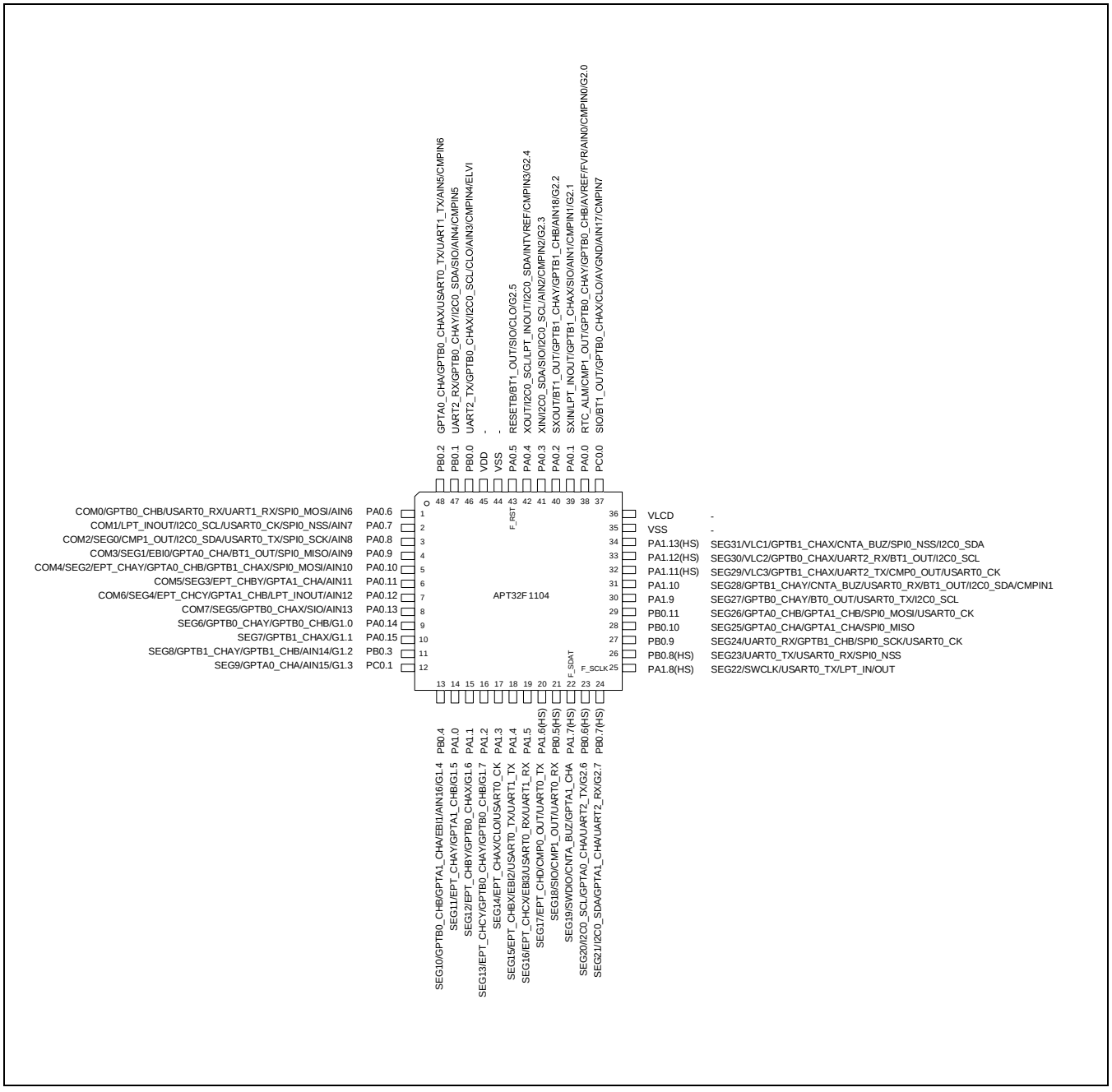


Figure 2-1 Pin definition diagram (48 LQFP)

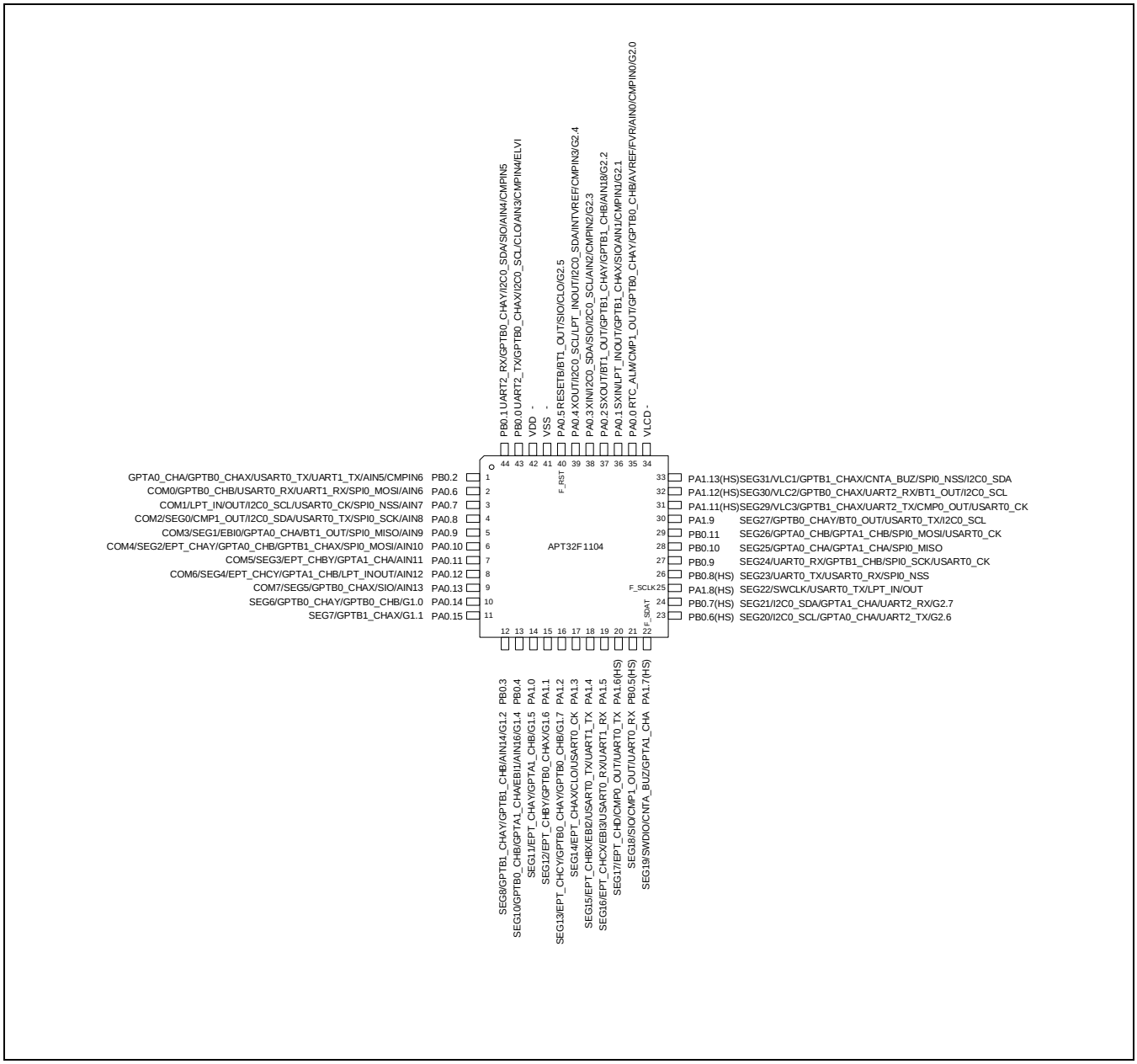


Figure 2-2 Pin definition diagram (44 QFP)

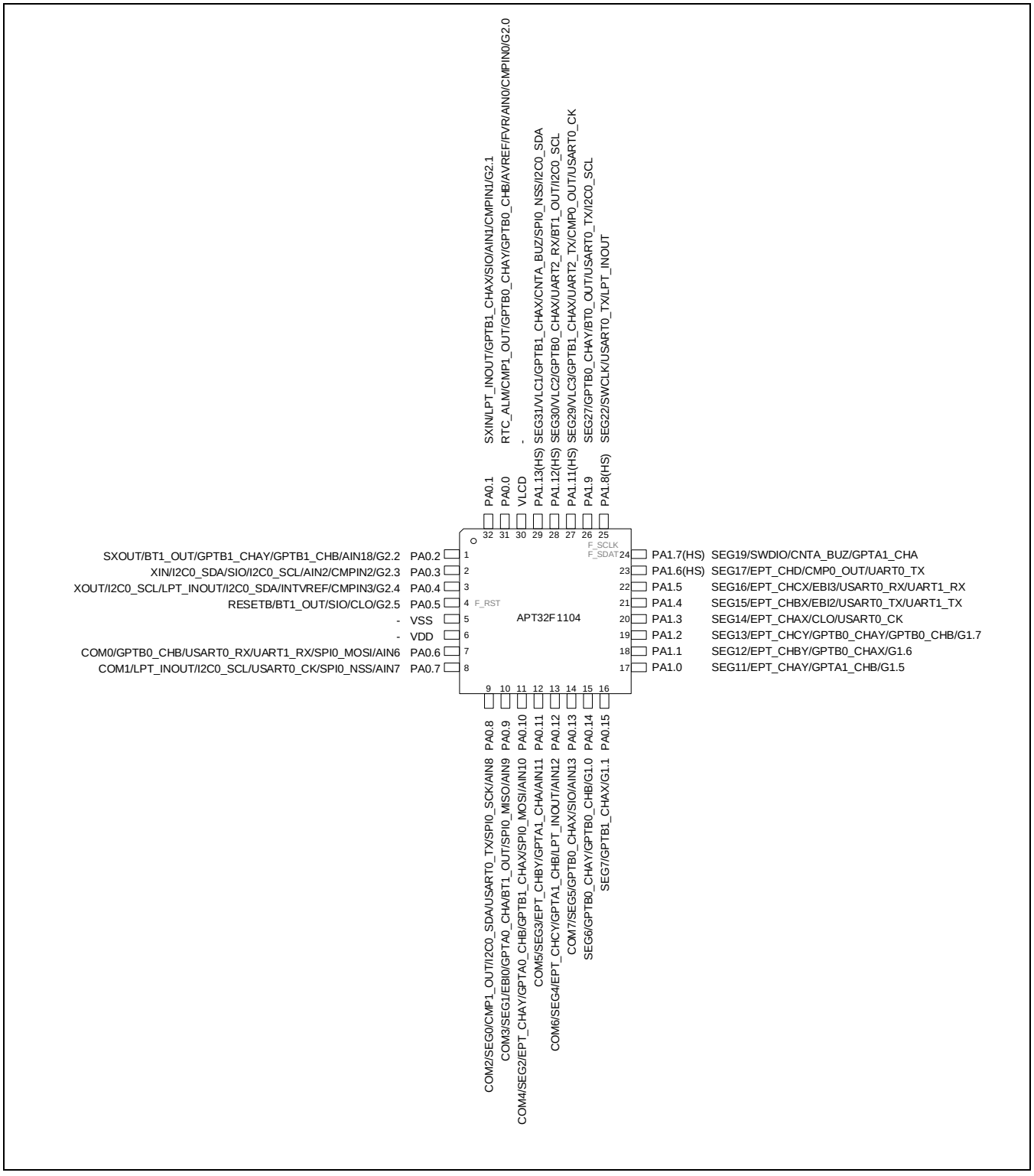


Figure 2-3 Pin definition diagram (32 LQFP/32 QFN)

2.3 Pin Function Allocation

Table 2-1 describes the detailed allocation of pin functions.

- *UP*: pull-up enable; *DN*: pull-down enable; *IO*: bidirectional; *I*: input; *O*: output; *P*: power; *G*: ground; *Z*: high impedance

Table 2-1 Pin Function Allocation

48LQFP	44QFP	32LQFP 32QFN	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	EXI	Default	PU/PD	Reset Status	Power Domain
36	34	30	VLCD	-	-	-	-	-	-	-	-	-	PWR	-	P	-
37	-	-	PC0.0	SIO	BT1_OUT	GPTB0_CHAX	CLO	-	AVGND	AIN17/CMPIN7	-	Y	IO	-	Z	RTE
38	35	31	PA0.0	RTC_ALM	CMP1_OUT	GPTB0_CHAY	GPTB0_CHB	-	-	AVREF/ FVR/AIN0/CMPIN0	G2.0	Y	IO	-	Z	ALV0
39	36	32	PA0.1	SXIN	LPT_INOUT	GPTB1_CHAX	SIO	-	-	AIN1	G2.1	Y	IO	-	Z	RTE
40	37	1	PA0.2	SXOUT	BT1_OUT	GPTB1_CHAY	GPTB1_CHB	-	-	AIN18	G2.2	Y	IO	-	Z	RTE
41	38	2	PA0.3	XIN	I2C0_SDA	SIO	I2C0_SCL	-	-	AIN2/CMPIN2	G2.3	Y	IO	-	Z	RTE
42	39	3	PA0.4	XOUT	I2C0_SCL	LPT_INOUT	I2C0_SDA	-	INTVREF	CMPIN3	G2.4	Y	IO	-	Z	RTE
43	40	4	PA0.5	-	BT1_OUT	SIO	CLO	-	-		G2.5	Y	IO	-	Z	ALV_R ESETB
44	41	5	VSS	-	-	-	-	-	-	-	-	-	GND	-	P	-
45	42	6	VDD	-	-	-	-	-	-	-	-	-	PWR	-	P	-
46	43	-	PB0.0	UART2_TX	GPTB0_CHAX	I2C0_SCL	CLO	-	-	AIN3/CMPIN4/ELVI	-	Y	IO	-	Z	ALV1
47	44	-	PB0.1	UART2_RX	GPTB0_CHAY	I2C0_SDA	SIO	-	-	AIN4/CMPIN5	-	Y	IO	-	Z	RTE
48	1	-	PB0.2	GPTA0_CHA	GPTB0_CHAX	USART0_TX	UART1_TX	-	-	AIN5/CMPIN6	-	Y	IO	-	Z	RTE
1	2	7	PA0.6	COM0	GPTB0_CHB	USART0_RX	UART1_RX	SPI0_MOSI		AIN6	-	Y	IO	-	Z	RTE
2	3	8	PA0.7	COM1	LPT_IN/OUT	I2C0_SCL	USART0_CK	SPI0_NSS		AIN7	-	Y	IO	-	Z	RTE
3	4	9	PA0.8	COM2/SEG0	CMP1_OUT	I2C0_SDA	USART0_TX	SPI0_SCK		AIN8	-	Y	IO	-	Z	RTE
4	5	10	PA0.9	COM3/SEG1	EBI0	GPTA0_CHA	BT1_OUT	SPI0_MISO		AIN9	-	Y	IO	-	Z	RTE
5	6	11	PA0.10	COM4/SEG2	EPT_CHAY	GPTA0_CHB	GPTB1_CHAX	SPI0_MOSI		AIN10	-	Y	IO	-	Z	RTE
6	7	12	PA0.11	COM5/SEG3	EPT_CHBY	GPTA1_CHA	-			AIN11	-	Y	IO	-	Z	RTE
7	8	13	PA0.12	COM6/SEG4	EPT_CHCY	GPTA1_CHB	LPT_INOUT			AIN12	-	Y	IO	-	Z	RTE
8	9	14	PA0.13	COM7/SEG5	GPTB0_CHAX	SIO	-			AIN13	-	Y	IO	-	Z	RTE
9	10	15	PA0.14	SEG6	GPTB0_CHAY	GPTB0_CHB	-		-		G1.0	Y	IO	-	Z	RTE
10	11	16	PA0.15	SEG7	GPTB1_CHAX	-	-		-		G1.1	Y	IO	-	Z	RTE
11	12	-	PB0.3	SEG8	GPTB1_CHAY	GPTB1_CHB	-		-	AIN14	G1.2	Y	IO	-	Z	RTE
12	-	-	PC0.1	SEG9	GPTA0_CHA	-	-		-	AIN15	G1.3	Y	IO	-	Z	RTE
13	13	-	PB0.4	SEG10	GPTB0_CHB	GPTA1_CHA	EBI1		-	AIN16	G1.4	Y	IO	-	Z	RTE
14	14	17	PA1.0	SEG11	EPT_CHAY	GPTA1_CHB	-		-		G1.5	Y	IO	-	I	RTE
15	15	18	PA1.1	SEG12	EPT_CHBY	GPTB0_CHAX	-		-		G1.6	Y	IO	-	I	RTE

48LQFP	44QFP	32LQFP 32QFN	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	EXI	Default	PU/PD	Reset Status	Power Domain
16	16	19	PA1.2	SEG13	EPT_CHCY	GPTB0_CHAY	GPTB0_CHB		-		G1.7	Y	IO	-	Z	ALV2
17	17	20	PA1.3	SEG14	EPT_CHAX	CLO	USART0_CK	-	-		-	Y	IO	-	Z	RTE
18	18	21	PA1.4	SEG15	EPT_CHBX	EBI2	USART0_TX	UART1_TX	-		-	Y	IO	-	Z	RTE
19	19	22	PA1.5	SEG16	EPT_CHCX	EBI3	USART0_RX	UART1_RX	-		-	Y	IO	-	Z	RTE
20	20	23	PA1.6 (HS)	SEG17	EPT_CHD	CMP0_OUT	UART0_TX		-		-	Y	IO	-	Z	RTE
21	21	-	PB0.5 (HS)	SEG18	SIO	CMP1_OUT	UART0_RX		-		-	Y	IO	-	Z	RTE
22	22	24	PA1.7 (HS)	SEG19	SWDIO	CNTA_BUZ	GPTA1_CHA		-		-	Y	SWDIO	UP	Z	ALV_SWDIO
23	23	-	PB0.6 (HS)	SEG20	I2C0_SCL	GPTA0_CHA	UART2_TX		-		G2.6	Y	IO	-	Z	RTE
24	24	-	PB0.7 (HS)	SEG21	I2C0_SDA	GPTA1_CHA	UART2_RX		-		G2.7	Y	IO	-	Z	RTE
25	25	25	PA1.8 (HS)	SEG22	SWCLK	USART0_TX	LPT_IN/OUT		-		-	Y	SWCLK	UP	Z	RTE
26	26	-	PB0.8 (HS)	SEG23	UART0_TX	USART0_RX	SPI0_NSS		-		-	Y	IO	-	Z	RTE
27	27	-	PB0.9	SEG24	UART0_RX	GPTB1_CHB	SPI0_SCK	USART0_CK	-		-	Y	IO	-	Z	RTE
28	28	-	PB0.10	SEG25	GPTA0_CHA	GPTA1_CHA	SPI0_MISO		-		-	Y	IO	-	Z	RTE
29	29	-	PB0.11	SEG26	GPTA0_CHB	GPTA1_CHB	SPI0_MOSI		USART0_CK		-	Y	IO	-	Z	ALV3
30	30	26	PA1.9	SEG27	GPTB0_CHAY	BT0_OUT	USART0_TX		I2C0_SCL		-	Y	IO	-	Z	RTE
31	-	-	PA1.10	SEG28	GPTB1_CHAY	CNTA_BUZ	USART0_RX	BT1_OUT	I2C0_SDA	CMPIN1	-	Y	IO	-	Z	RTE
32	31	27	PA1.11(HS)	SEG29/VLC3	GPTB1_CHAX	UART2_TX	CMP0_OUT		USART0_CK		-	Y	IO	-	Z	RTE
33	32	28	PA1.12(HS)	SEG30/VLC2	GPTB0_CHAX	UART2_RX	BT1_OUT		I2C0_SCL		-	Y	IO	-	Z	RTE
34	33	29	PA1.13(HS)	SEG31/VLC1	GPTB1_CHAX	CNTA_BUZ	SPI0_NSS		I2C0_SDA		-	Y	IO	-	Z	RTE
35	-	-	VSS	-	-	-	-	-	-	-	-	-	GND	-	P	-

Note：

(1) The external reset function is multiplexed with the PA0.5 pin, you can use the User Option function to select the configuration

(2) F_SCLK, F_SDAT, F_RSTB are the interface signals of the external flash memory burning tool

(3) As long as each IO pin is configured as a digital IO function, the EXI function can be used to trigger an interrupt

(4) The IO marked with the (HS) symbol is a high current drive port (High Sink Current IO), which supports a sink current of 120mA. For the configuration method, please refer to the GPIO chapter

(5) AF8 G1/G2 is the IO redefinition function, you can freely define the AF function of IO, the specific configuration method refers to the IO redefinition in the SYSCON chapter

(6) In the Power Down column, RET indicates that when entering the shutdown low power mode, the chip latches and maintains the current IO control. ALV*: After the chip enters the shutdown low-power mode, if the corresponding pin has been configured as a wake-up source, this pin can wake up the chip. For details, please refer to the shutdown low-power mode wake-up in the SYSCON chapter

2.4 Function Pin Mapping

The related functions of each peripheral can be selected through the AF function setting of GPIO. Some multiplexed functions have remapped pins, which is convenient for users to use various functions in various applications

Note：

(1) For the output function, if multiple pins are configured to the same function, then all these pins will output the same signal

(2) For input function, if multiple pins are configured to the same function, the pin with the smaller AF number has higher priority. For example, when both PA0.05 and PA0.9 are configured as UART0_RXD, only PB0.05(AF4) is UART0_RXD, and the UART0_RXD configuration of PB0.9(AF2) is invalid

(3) G1/G2 is the IO redefinition function. On the basis of the original AF0~AF8, it also provides additional free definition functions. For the specific configuration method, please refer to the IO redefinition in the SYSCON chapter

2.5 Pin Function Description

This paragraph describes the functions of the following pins:

- Power pin
- System function pins
- Common module function pins
- Debug interface pins
- Flash burning tool pins

Note：

(1) D: digital; A: analog

(2) I/O: bidirectional; I: input; O: output

(3) P: power supply; G: ground

(4) Z: high impedance

2.5.1 Power Pin

Table 2-2 Power Pin Description

Module	Pin Name	I/O	Pin Description	D/A
Power	VDD	-	Chip power	-
	VSS	-	Chip ground	-
	VLCD	-	LCD power supply	

2.5.2 System Function Pins

Table 2-3 System Function Pin Description

Module	Pin Name	I/O	Pin Description	D/A
System	RESETB	I	Hardware reset input	D
	XIN	I	External main crystal oscillator input	A
	XOUT	O	External main crystal oscillator output	A
	SXIN	I	External secondary crystal oscillator (RTC crystal oscillator) input	A
	SXOUT	O	External secondary crystal oscillator (RTC crystal oscillator) output	A
	CLO	O	Internal system clock output	D

2.5.3 Common Module Function Pins

Table 2-4 Common Module Function Pin Description

Module	Pin Name	I/O	Pin Description	D/A
GPIO	PA0.x	I/O	General IO A0	D
	PA1.x	I/O	General IO A1	D
	PB0.x	I/O	General IO B0	D
	PC0.x	I/O	General IO C0	D
EPT	EPT_CHAX	O	X output of channel A of EPT	D
	EPT_CHAY	O	Y output of channel A of EPT	D
	EPT_CHBX	O	X output of channel B of EPT	D
	EPT_CHBY	O	Y output of channel B of EPT	D
	EPT_CHCX	O	X output of channel C of EPT	D
	EPT_CHCY	O	Y output of channel C of EPT	D
	EPT_CHD	O	Channel D output of EPT	D
	EBIx	I	EPT emergency trigger signal	D
GPTA	GPTAx_CHA	O	Channel A output of GPTA	D
	GPTAx_CHB	O	Channel B output of GPTA	D
GPTB	GPTBx_CHAX	O	X output of channel A of GPTB	D
	GPTBx_CHAY	O	Y output of channel A of GPTB	D
	GPTBx_CHB	O	Channel B output of GPTB	D
BT	BTx_OUT	O	BT output	D
CNTA	CNTA_BUZ	O	Carrier frequency output of counter A	D
LPT	LPT_OUT	O	Waveform output of LPT	D
	LPT_IN	I	External input of LPT	D
RTC	RTC_ALM	O	RTC timing pulse output	D
I2C	I2C_SCL	I	I2C serial clock	D
	I2C_SDA	I/O	I2C serial data	D
UART	UARTx_RX	I	UART serial data reception	D
	UARTx_TX	O	UART serial data transmission	D
USART	USARTx_RX	I	UART serial data reception	D
	USARTx_TX	O	UART serial data transmission	D
	USARTx_CK	O	USART CK output	D
SPI	SPI_NSS	I/O	SPI chip select signal	D
	SPI_SCK	I/O	SPI synchronous clock signal	D
	SPI_MOSI	O	SPI data output port	D

	SPI_MISO	I	SPI data input port	D
SIO	SIO	I/O	SIO data input and output port	D
ADC	AINx	I	ADC analog input channel	A
	AVREF	I	ADC external reference voltage input signal	A
LVD	LVDIN	I	LVD input comparison voltage	A
LCD	COM[1:0]	O	LCD segment (panel) common terminal drive signal	A
	COM[7:2]/SEG[5:0]	O	voltage level for COM driver signal	A
	SEG[28:6]	O	LCD segment (panel) common/segment side drive signal	A
	VLC3/SEG29	O	Appropriate voltage level for COM/SEG driver signal	A
	VLC2/SEG30	O	LCD segment (panel) segment side drive signal	A
	VLC1/SEG31	O	Appropriate voltage level for SEG driver signal	A
CMP	CMPx_OUT	O	CMP comparison result output	D
	CMPINx	I	CMP analog input	A

2.5.4 Debug Interface Pins

Table 2-5 Debug Interface Pin Description

Module	Pin Name	I/O	Pin Description	D/A
SWD	SWCLK（PA1.8）	I	Serial clock, internal pull-up	D
	SWDIO（PA1.7）	I/O	Serial data input/output, internal pull-up	D

2.5.5 Pins Of Flash Programming Tool

Table 2-6 Pin Description of Flash Burning Tool

Module	Pin Name	I/O	Pin Description	D/A
FLASH	F_SCL	I	Serial clock	D
	F_SDA	I/O	Serial data	D
	RSTB	I	Reset	D
	VDD	P	Power supply (It is recommended to connect a 0.1uF decoupling capacitor between VDD and VSS)	A
	VSS	G	Ground	A

3 Electrical Characteristics

3.1 Limit Parameters

If the device exceeds the following “limit parameters”, it may cause permanent damage. The device can only be guaranteed to work normally within the range of conditions specified in the manual. Working under the "limit parameter" condition will affect the reliability of the device.

Table 3-1 Limit Parameters

Parameter	Symbol	Condition	Value	Unit
Operating Voltage	V_{DD}	–	–0.3 to 6.5	V
Input voltage	V_{IN}	–	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O	All ports	–0.3 to V_{DD} + 0.3	V
IO drive current	I_{SINK1}	Ordinary port IO injection	15	mA
		Strong pull-down driver port	120	mA
	I_{SINK2}	All IO injection	200	mA
	I_{SOURCE}	Single IO pull	15	mA
Working temperature	T_A	–	–40 to 85	°C
Storage temperature	T_{STG}	–	–65 to 150	°C

3.2 Recommended Working Conditions

The device needs to work under the recommended operating conditions. The electrical characteristic parameters listed in this chapter need to be guaranteed under the recommended conditions. The device's working conditions beyond the recommended conditions may reduce its reliability and even cause damage to the device.

Table 3-2 Recommended Working Conditions

Parameter	Symbol	Condition	Value	Unit
Operating Voltage	V_{DD}	–	1.8 to 5.5	V
Working temperature	T_A	–	–40 to 85	°C

3.3 I/O Port Characteristics

Table 3-3 I/O Port Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Input high voltage	V_{IH}	All ports	0.8 V_{DD}	–	V_{DD}	V
Input low voltage	V_{IL}	All ports	–	–	0.2 V_{DD}	V
Output high voltage	V_{OH}	I_{OH} = -15mA, V_{DD} = 5V	V_{DD} – 1.0	–	–	V
Output low voltage	V_{OL1}	I_{OL1} = 15mA , V_{DD} = 5V (All ports)	–	–	1	V
	V_{OL2}	I_{OL2} = 120mA , V_{DD} = 5V (PA1.6 ~ PA1.8, PA1.11 ~ PA1.13, PB0.5 ~ PB0.8 Strong pull-down drive mode)	–	–	1	V
Constant current drive current	I_{OC}	V_{DD} = 5V, V_{OH} < 4V (PA0.6 ~ PA0.15, PA1.0 ~ PA1.2, PB0.3, PB0.4, PC0.1 Constant current source mode)	–	10	–	mA
High input leakage current	I_{LIH}	All ports, V_{IN} = V_{DD}	–	–	1	uA
Low input leakage current	I_{LIL}	All ports, V_{IN} = 0	–	–	–1	uA
Pull-up resistor	R_{PU}	V_{DD} = 5V, V_{IN} = 0V	25	50	75	kΩ
Pull-down resistor	R_{PD}	V_{DD} = 5V, V_{IN} = 5V	25	50	75	kΩ

3.4 I/O Port AC Characteristics

Table 3-4 I/O Port AC Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Input the maximum frequency	IOF_{IN}	All ports	–	10	–	MHz
Output the maximum frequency	IOF_{OUT}	All ports	–	10	–	MHZ

3.5 Input Reset Characteristics

Table 3-5 Input Reset Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Minimum low voltage pulse width	T_{NRST}	–	100	300	500	nS
nRESET Hysteresis voltage	V_{hyst}	Rise and fall	–	1	–	V

NOTE： The filter width of the input reset signal is 100 ns to 500 ns.
If the width of the input reset signal is less than 100 ns, it will be regarded as an invalid signal (not reset).
If the width of the input reset signal is higher than 500 ns, it will be regarded as a valid signal (reset).

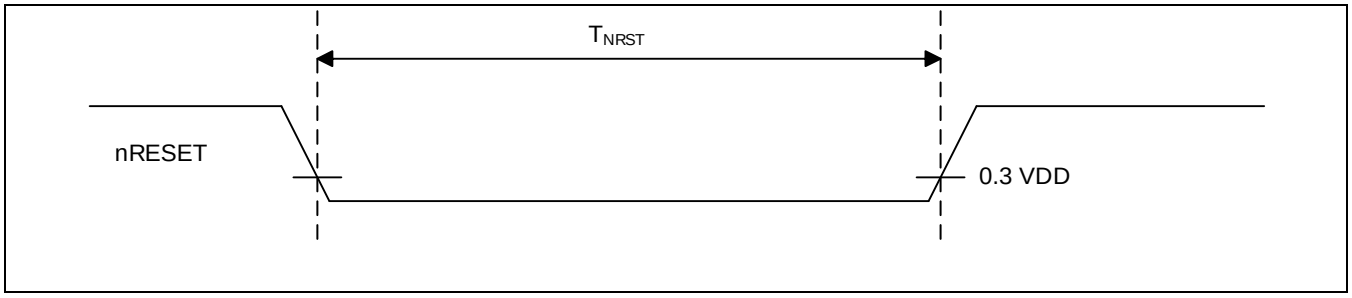


Figure 3-1 nRESET Input timing

3.6 Power-on and Power-down Reset Characteristics

Table 3-6 Power-on and Power-down Reset Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Power-on power change rate	SR_{VDD}	–	0.1	–	–	V/mS

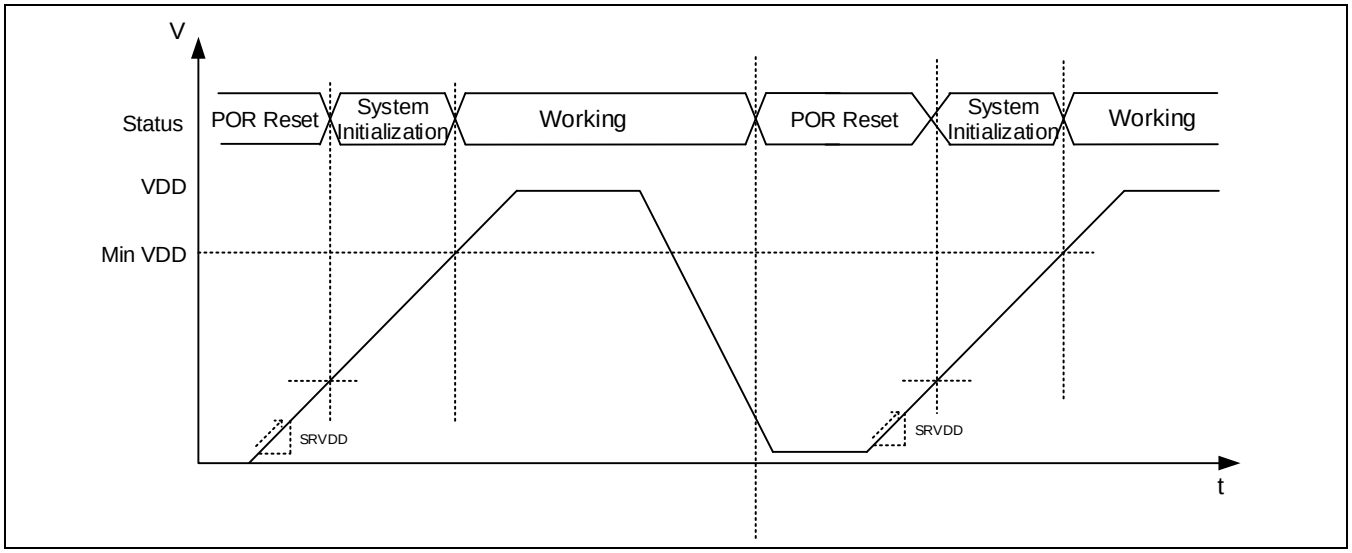


Figure 3-2 Schematic diagram of power-on and power-down

3.7 External Interrupt Input Characteristics

Table 3-7 External Interrupt Input Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Interrupt input high pulse width	t_{INTH}	V_{DD} = 5.0V	15	30	45	nS
Interrupt input low pulse width	t_{INTL}	V_{DD} = 5.0V	15	30	45	nS

NOTE：The filter width of the input reset signal is 15 ns to 45 ns.
If the width of the input reset signal is less than 15 ns, it will be regarded as an invalid signal.
If the width of the input reset signal is higher than 45 ns, it will be regarded as a valid signal.

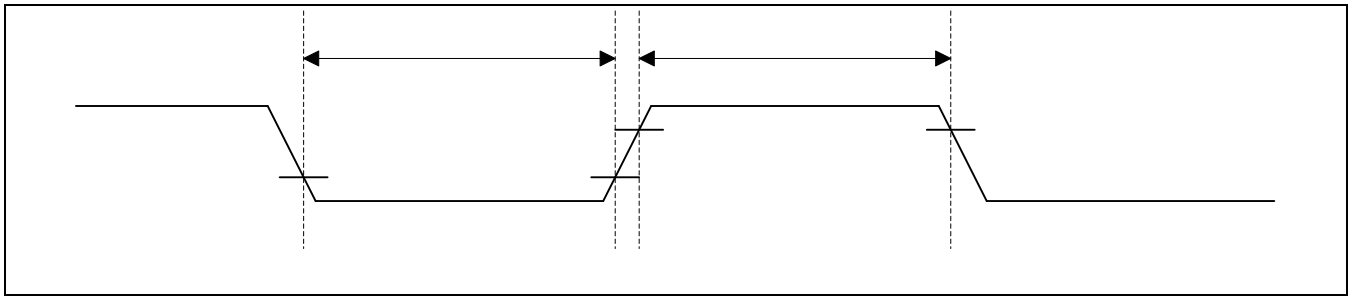


Figure 3-3 External interrupt input timing

3.8 Oscillator Characteristics

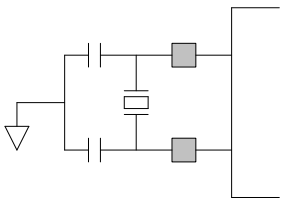
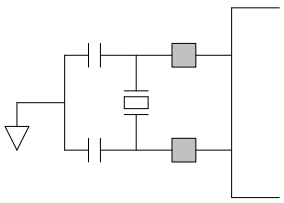
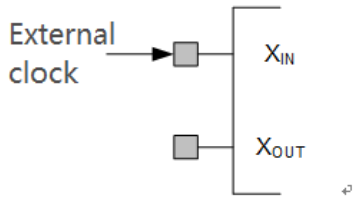
Five types of oscillators are included in the system:

- External main oscillator
- External sub-oscillator
- Internal main oscillator
- Internal high-speed oscillator
- Internal sub-oscillator

3.8.1 External Main Oscillator

Table 3-8 External Main Oscillator Characteristics

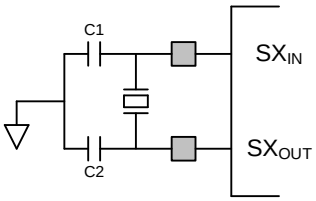
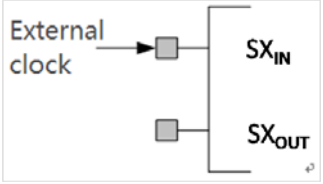
(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Oscillator frequency	F_{EMOSC}	–	0.4	–	24	Mhz
Internal feedback resistance	R_{FD}	XIN Port	2	4	10	MΩ
stable schedule	T_{STA}	–	–	20	–	ms
External crystal oscillator (normal mode)	–		0.4	–	24	MHz
External crystal oscillator (low frequency mode)	–		–	32.768	–	KHz
External clock	–		0.4	–	24	MHz

3.8.2 External Sub-oscillator

Table 3-9 External Sub-oscillator Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Oscillator frequency	F_{ESOSC}	–	–	32.768	–	Khz
Internal feedback resistance	R_{FD}	SXIN Port	–	9.5	–	MΩ
stable schedule	T_{STA}	–	–	900	–	ms
External crystal oscillator	–		–	32.768	–	Khz
External clock	–		–	32.768	–	Khz

3.8.3 Internal Main Oscillator Characteristics

Table 3-10 Internal Main Oscillator Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Oscillator frequency	F_{IMOSC}	IM0	–	5.556	–	MHz
		IM1	–	4.194	–	MHz
		IM2	–	2.097	–	MHz
		IM3	–	131.072	–	KHz
Duty cycle	T_{OD}	–	40	50	60	%
Accuracy after calibration	T_{ACC}	T_A = 27°C	-1	–	+1	%
		IM0 T_A = –40 to 85°C	-4	–	+3	%
		IM1 T_A = –40 to 85°C	-4	–	+3	%
		IM2 T_A = –40 to 85°C	-4	–	+3	%
		IM3 T_A = –40 to 85°C	-6	–	+5	%
Stable schedule	T_{STA}	After the supply voltage reaches the minimum operating value	–	–	10	Clk

3.8.4 Internal High-speed Oscillator Characteristics

Table 3-11 Internal High-speed Oscillator Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Oscillator frequency	F_{IMOSC}	–	–	48	–	Mhz
Duty cycle	T_{OD}	–	40	50	60	%
Accuracy after calibration	T_{ACC}	T_A = 27°C	-1	–	+1	%
		T_A = –40 to 85°C	-4	–	+4	%
Stable schedule	T_{STA}	After the supply voltage reaches the minimum operating value	–	–	10	Clk

3.8.5 Internal Sub-oscillator Characteristics

Table 3-12 Internal Sub-oscillator Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Oscillator frequency	F_{ISOSC}	–	–	27	–	KHz
Duty cycle	T_{OD}	–	40	50	60	%
Precision	T_{ACC}	T_A = 27°C	-1	–	+1	%
		T_A = –40 to 85°C	-9	–	+6	%
Stable schedule	T_{STA}	After the supply voltage reaches the minimum operating value	–	–	10	Clk

3.9 Working Current

Table 3-13 Working Current

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	State name	Condition	Minimum value	Typical value	Typical value	Unit
Working current	I_{DD1}	RUN 1	V_{DD} = 5.0V , T_A =25°C CPU = 48MHz	–	10	–	mA
		RUN 2	V_{DD} = 5.0V , T_A =25°C CPU = 5.556MHz	–	4	–	mA
		RUN 3	V_{DD} = 5.0V , T_A =25°C CPU = 131KHz	–	0.5	–	mA
	I_{DD2}	SLEEP 1	V_{DD} = 5.0V , T_A =25°C CPU = 48MHz	–	1	–	mA
		SLEEP 2	V_{DD} = 5.0V , T_A =25°C CPU = 5.556MHz	–	0.2	–	mA
		SLEEP 3	V_{DD} = 5.0V , T_A =25°C CPU = 131KHz	–	0.1	–	mA
	I_{DD3}	DEEP-SLEEP1	V_{DD} = 5.0V , T_A =25°C	–	10	TBD	uA
		DEEP-SLEEP2	VDD = 1.8V to 5.5V , TA = –40 to 85°C	–	–	TBD	uA
	I_{DD4}	SNOOZE 1	V_{DD} = 5.0V , T_A =25°C w/o LCD	–	7	TBD	uA
		SNOOZE 2	VDD = 1.8V to 5.5V TA = –40 to 85°C w/o LCD	–	–	TBD	uA
		SNOOZE 3	V_{DD} = 3.3V , T_A =25°C w/o LCD	–	6	–	uA
		SNOOZE 4	V_{DD} = 3.3V , T_A =25°C w/t LCD	–	9	–	uA
	I_{DD5}	SHUTDOWN1	V_{DD} = 5.0V ,T_A = 25°C w/o RTC(ESOSC)	–	1.5	TBD	uA
		SHUTDOWN2	VDD = 1.8V to 5.5V TA = –40 to 85°C w/o RTC(ESOSC)	–	–	TBD	uA
		SHUTDOWN3	V_{DD} =5.0V , T_A =25°C w/t RTC(ESOSC)	–	3.0	–	uA

NOTE: **The operating current does not include the pull-up and pull-down current of the I/O port.**

3.10 Low-voltage Reset Monitoring Characteristics

Table 3-14 Low-voltage Reset Monitoring Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Low voltage reset voltage (VDD falling edge)	Vthrf	–	1.8	1.9	2.0	V
		–	2.1	2.2	2.3	
		–	2.4	2.5	2.6	
		–	2.7	2.8	2.9	
		–	2.95	3.1	3.25	
		–	3.25	3.4	3.55	
		–	3.55	3.7	3.85	
		–	3.85	4.0	4.15	
Low voltage monitoring voltage (VDD falling edge)	Vthdf	–	2.0	2.1	2.2	
		–	2.3	2.4	2.5	
		–	2.6	2.7	2.8	
		–	2.85	3.0	3.15	
		–	3.15	3.3	3.45	
		–	3.45	3.6	3.75	
		–	3.75	3.9	4.05	
		–	0.9	1.0 (LVDIN)	1.1	
Hysteresis voltage	ΔV_{LVD}	–	–	200	–	mV
Working current	I_{CC}	–	–	9	–	uA
Shutdown current	I_{PD}	–	–	0.1	–	uA

3.11 12 Bit A/D Converter Characteristics

Table 3-15 12 Bit A/D Converter Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Precision	–	–	–	12	–	Bit
Operating Voltage	V_{ADC}	–	1.8(1)	5	5.5	V
Reference reference voltage	V_{REF}	V_{REF} <V_{ADC}	2	5	5.5	V
Input voltage range	V_{AIN}	–	0	–	V_{REF}	V
Conversion rate	F_S	–	–	–	1	MHz
Differential nonlinearity	DNL	F_S = 0.5MHz V_{ADC} = 5V	–	-	±2.0	LSB
Integral nonlinearity	INL		–	-	±4.0	
Offset error	TOPOFF		–	-	±10.0	
	BOTOFF		–	-	±10.0	
Working current	I_{OP}	–	–	1	–	mA
Shutdown current	I_{PD}	–	–	1	–	μA
ADC clock frequency	F_{ADC}	–			24	MHz
ADC conversion period	T_{conv}	T_{sample} = 8		24		T_{ADC}
External input impedance	R_{AIN}(2)	F_{ADC} = 1MHz V_{ADC} = 5V T_{sample} = 8			50	K

NOTE： The above data are application evaluation results, not mass production test results.

(1) ADC speed is limited when working under low voltage. When working at 1.8V, the ADC clock frequency should be less than 500 KHz.

(2) The input impedance of the ADC is related to the working clock frequency and the number of sampling cycles. CADC is the internal sample and hold capacitor, the charging time of this capacitor needs to meet TC=10 x (RADC+RAIN) x CADC. Among them, RADC is the sampling switch resistance, the maximum value is 1 K; CADC is the internal sampling and holding capacitor, the maximum value is 5 pF.

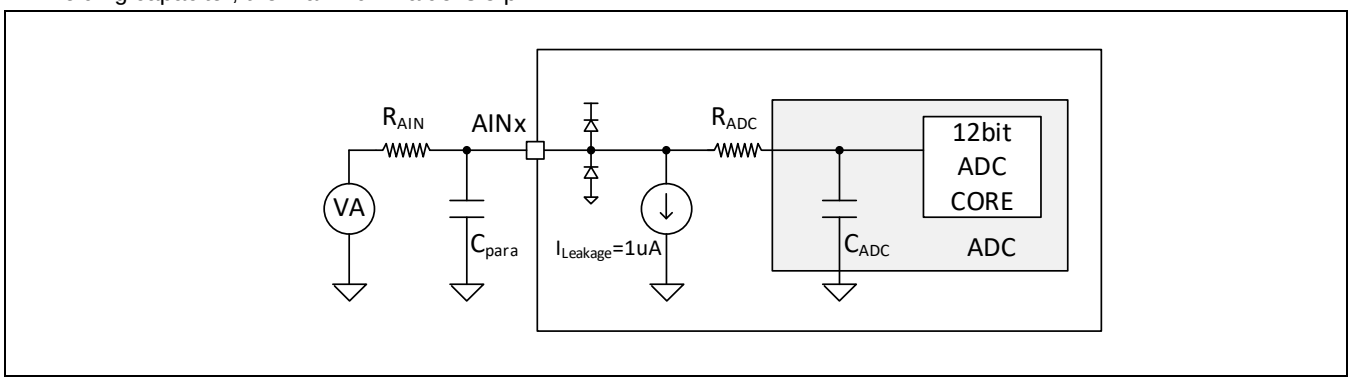


Figure 3-4 ADC Sample connection diagram

3.12 Internal Fixed Reference Voltage Characteristics

Table 3-16 Internal Fixed Reference Voltage Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Low reference voltage	FVR_L	$V_{DD} > FVR_L$	–	2.048	–	V
High reference voltage	FVR_H	$V_{DD} = FVR_H$	–	4.096	–	V
Low reference voltage accuracy	Vaccl1	V_{DD} = 5.0V T_A = 25°C	-1%	2.048	1%	V
	Vaccl2	V_{DD} > 2.7V T_A = –40 to 85°C	–	2.048	2%	V
High reference voltage accuracy	Vacch1①	V_{DD} = 5V T_A = 25°C	-1%	4.096	1%	V
	Vacch2②	V_{DD} = 5V T_A = –40 to 85°C	–	4.096	2%	V

3.13 Internal INTVREF Reference Voltage Characteristics

Table 3-17 Internal INTVREF Reference Voltage Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
INTVREF Reference voltage	$V_{INTVREF}$	–	–	1.0	–	V
INTVREF Precision	Vacc1	T_A = 25°C	–1%	1.0	1%	V
	Vacc2	T_A = –40 to 85°C	–2%	1.0	2%	V

3.14 Comparator Characteristics

Table 3-18 Comparator Characteristics

(T_A = –40 to 85°C, V_{DD} = 2.4V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Input offset voltage	V_{OFF}	–	–	1	TBD	mV
Input common mode voltage	V_{ICM}	–	0	–	V_{DD}	V
Response time(1)	T_{RESP}	Differential input 10mV	–	1	–	uS
		Differential input 100mV		0.5		
Hysteresis voltage	V_{HYST}	Mode 0	–3	0	3	mV
		Mode 1	3	5	8	
		Mode 2	6	10	13	
		Mode 3	12	15	18	
		Mode 4	17	20	23	
		Mode 5	21	25	28	
		Mode 6	37	40	45	
		Mode 7	55	60	65	

NOTE: (1) It is the response time of the comparator itself. If the subsequent digital filter is turned on, the delay of the digital filter needs to be increased. Refer to Comparator.

3.15 LCD Characteristics

Table 3-19 LCD Characteristics

(T_A = –40 to 85°C, V_{DD} = 2.0V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
VLCD external CAP	Cvlcd	When using the internal boost source	0.1	1	2	uF
Internal boost source output	Vcp	VLCDS = 0b111	–	4	–	V
		VLCDS = 0b110	–	3.8	–	
		VLCDS = 0b101	–	3.6	–	
		VLCDS = 0b100	–	3.4	–	
		VLCDS = 0b011	–	3.2	–	
		VLCDS = 0b010	–	3.0	–	
		VLCDS = 0b001	–	2.8	–	
		VLCDS = 0b000	–	2.6	–	
Drive resistance	Rdrv(1)	HD_EN=1，HDPULSE_ EN=1	–	60K	–	Ω
		HD_EN=0，HDPULSE_ EN=1	–	240K	–	
		HD_EN=0，HDPULSE_ EN=0	–	7M	–	

NOTE: (1) For driving resistance (Rdrv), please refer to LCD controller chapter. When R_L is used, the internal charge pump can no longer guarantee the driving capability. Therefor external VLCD is suggested.

(2) Internal boost is limited by power supply VDD，V_{CPMAX}= 2*VDD -0.6 (Example VDD=2.1V，V_{CPMAX} = 3.6V)。

3.16 Memory Characteristics

Table 3-20 RAM and Register Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Data retention voltage (1)	V_{DDDR}	Deep sleep mode	0.8	–	V_{DD}	V

NOTE: (1) The lowest voltage value to ensure that the data in the RAM is not lost (in deep sleep mode), or the lowest voltage value to maintain the state of the register (in deep sleep mode). Guaranteed by design, not tested in mass production.

Table 3-21 FLASH Memory Characteristics

(T_A = –40 to 85°C, V_{DD} = 1.8V to 5.5V)

Parameter	Symbol	Condition	Minimum value	Typical value	Maximum value	Unit
Programming size	F_{WSIZE}	–	–	4	–	Byte
Page size	F_{PSIZE}	–	–	1024	–	Byte
Programming time (1Word)	F_{tprog}	–	20	–	–	us
Page erase time	F_{tpera}	–	2	–	–	ms
Full chip erasing time	F_{tmera}	–	10	–	–	ms
DROM Programming times	F_{dnwe}	Each Page	100,000	–	–	Times
PROM Programming times	F_{pnwe1}	Each Page	100,000	–	–	Times
PROM Programming Total times (1)	F_{pnwe2}		–	–	200,000	Times
Data retention time	F_{tdr}	–	10	–	–	Years
Power consumption (when programming or erasing)	F_{idd}	–	–	–	5	mA

NOTE(1)：Each page erase or chip erase counts one.

3.17 Electrostatic Discharge (ESD) Characteristics

Table 3-22 Electrostatic Discharge Characteristics

Parameter	Symbol	model	Minimum value	Typical value	Maximum value	Unit
Static protection withstand voltage	V_{ESD}	HBM	4000	–	–	V
		MM	200	–	–	V
		CDM	500	–	–	V

4 Package Size

4.1 APT32F1104 Support Package Type

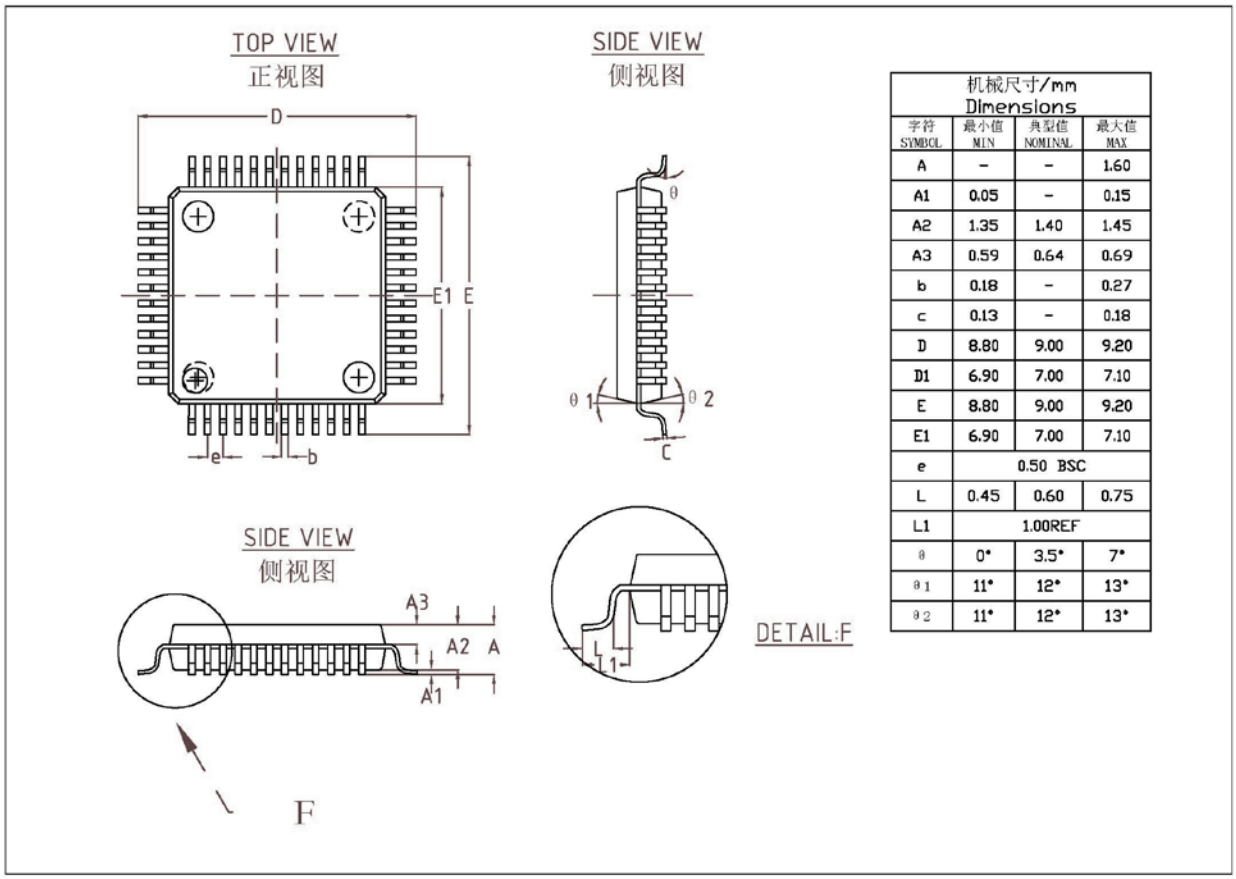
LQFP48

QFP44

LQFP32

QFN32

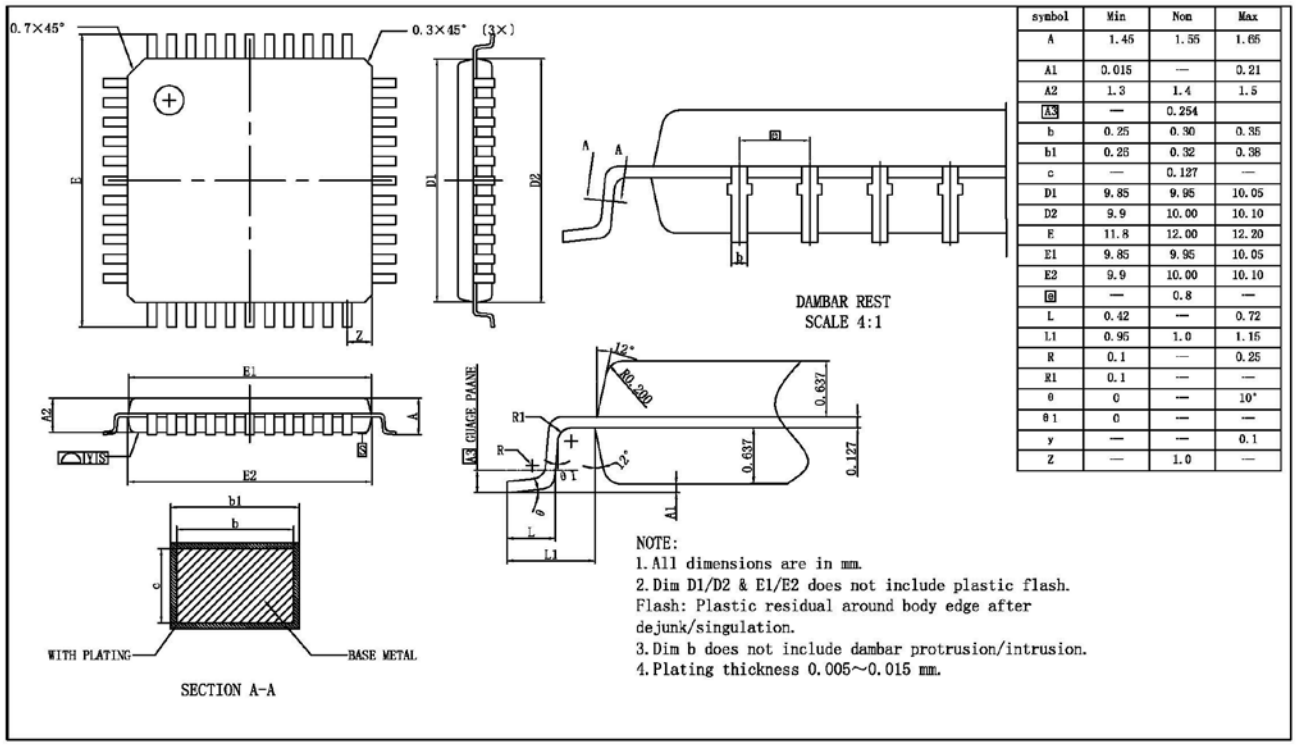
4.2 LQFP48



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
c	0.13	–	0.18
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

Figure 4-1 LQFP48 (7x7-0.5mm) Package size

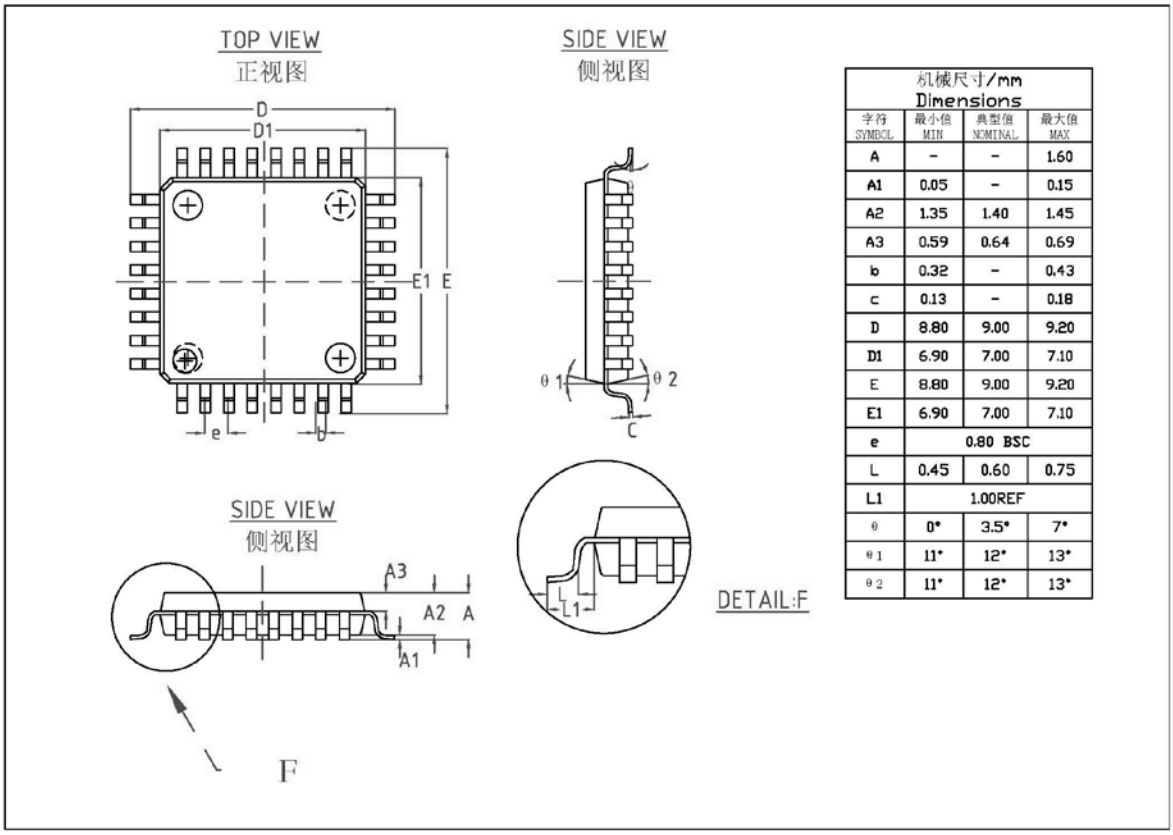
4.3 QFP44



symbol	Min	Nom	Max
A	1.45	1.55	1.65
A1	0.015	—	0.21
A2	1.3	1.4	1.5
A3	—	0.254	
b	0.25	0.30	0.35
b1	0.25	0.32	0.38
c	—	0.127	—
D1	9.85	9.95	10.05
D2	9.9	10.00	10.10
E	11.8	12.00	12.20
E1	9.85	9.95	10.05
E2	9.9	10.00	10.10
e	—	0.8	—
L	0.42	—	0.72
L1	0.95	1.0	1.15
R	0.1	—	0.25
R1	0.1	—	—
θ	0	—	10°
θ1	0	—	—
y	—	—	0.1
Z	—	1.0	—

Figure 4-2 QFP44 (10x10-0.8mm) Package size

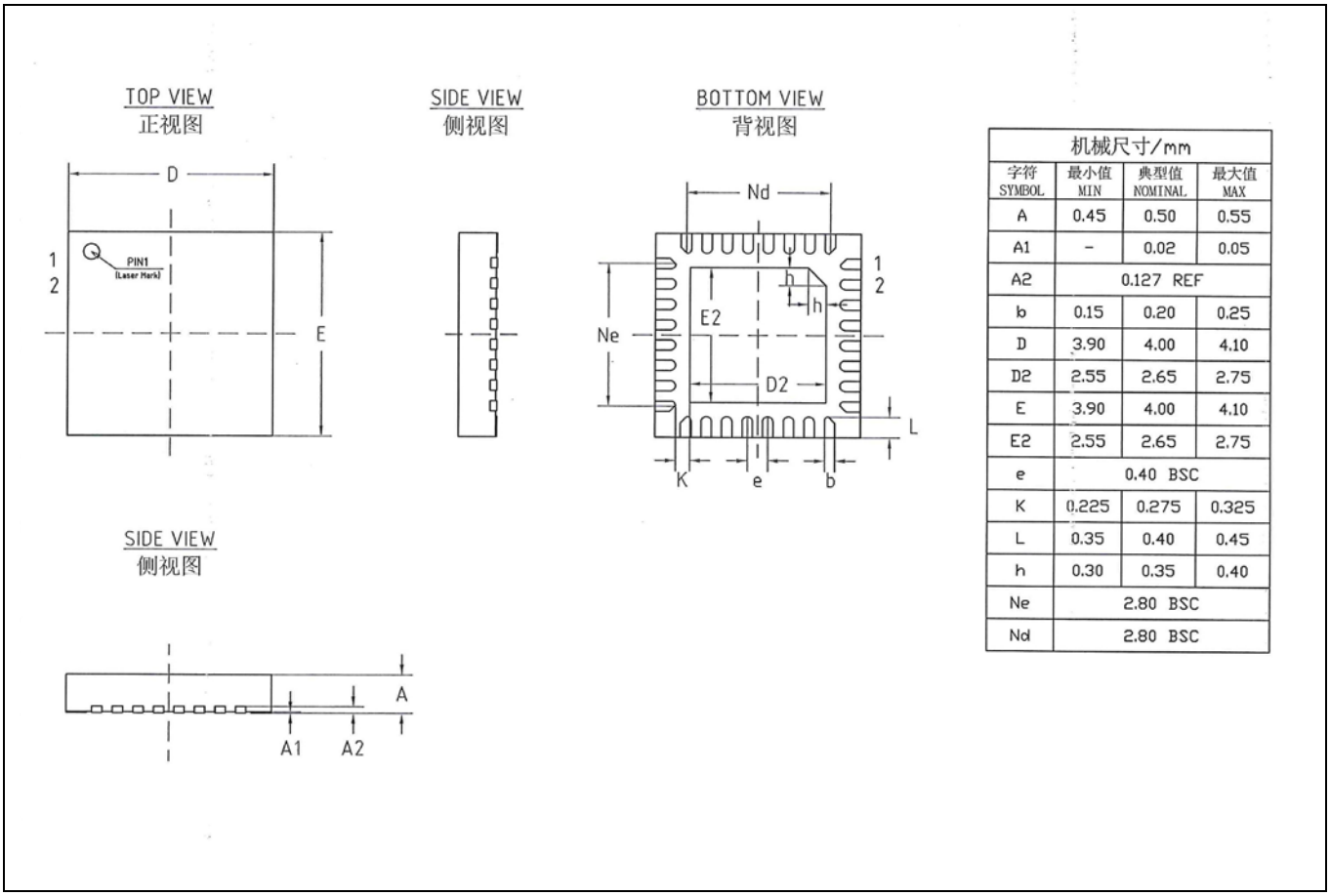
4.4 LQFP32



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	-	0.43
c	0.13	-	0.18
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.80 BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

Figure 4-3 LQFP32 (0.8mm) Package size

4.5 QFN32



机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	0.45	0.50	0.55
A1	-	0.02	0.05
A2	0.127 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.55	2.65	2.75
E	3.90	4.00	4.10
E2	2.55	2.65	2.75
e	0.40 BSC		
K	0.225	0.275	0.325
L	0.35	0.40	0.45
h	0.30	0.35	0.40
Ne	2.80 BSC		
Nd	2.80 BSC		

Figure 4-4 QFN32 (4x4, 0.4mm) Package size

5 Ordering Information

5.1 Product Naming Rules

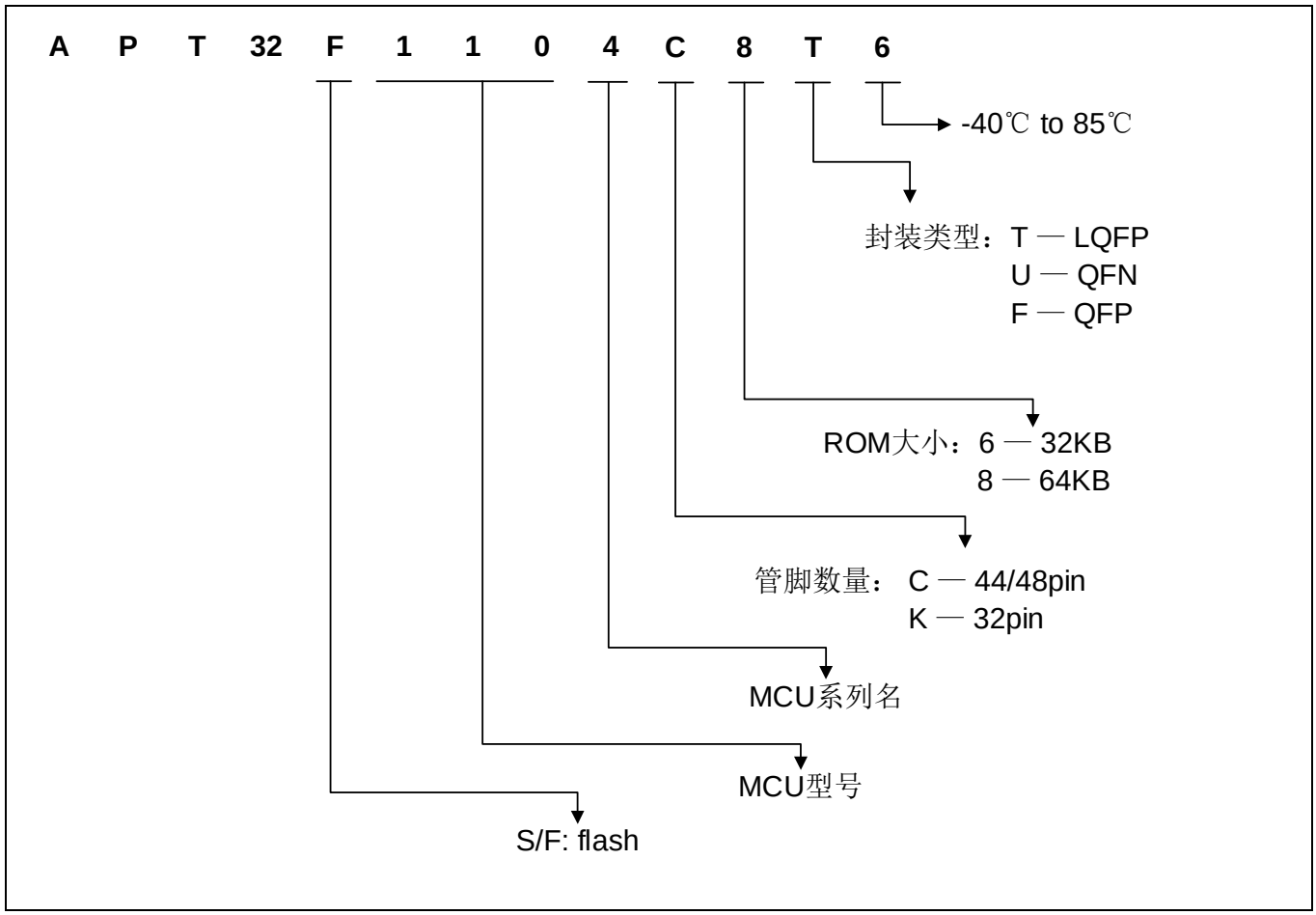


Figure 5-1 Product naming rules

5.2 Series Product Order Model

Table 5-1 APT32F1104 Product Order Model Description

Series	Model details
1104	APT32F1104C8T6/APT32F1104C6T6 APT32F1104C8F6/APT32F1104C6F6 APT32F1104K8T6/APT32F1104K6T6 APT32F1104K8U6/APT32F1104K6U6