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SPECIFICATION

MODULE NO	VL128649A-WP
VERSION	A
CUSTOMER	
APPROVE by	

Sale by	Check by	Prepare by
SALES 2017.02.22 Tommy	RD 2017.02.22 Lame	RD 2017.02.22 Emma

INDEX

ISSUE RECORD

NO.	VER.	DATE	MODIFY REASON	MODIFY CONTENTS
1	A	2017/02/21	New issued	

1. General Specification

1.1 Mechanical Dimension

Item	Dimension	Unit
Number of Dots	128 x 64	dots
Module dimension (L x W x H)	26.7 x 61.26 x 1.41(Without component)	mm
View area	23.74 x 12.864	mm
Active area	21.744 x 10.864	mm
Dot size	0.17(W) x 0.17(H)	mm
Dot pitch	0.186(W) x 0.186(H)	mm
Color	White	
Interface	68xx 8bit	

1.2 Controller IC: SSD1306BZ Controller

2. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	—	+70	℃
Storage Temperature	TST	-40	—	+85	℃
Humidity		—	—	85	%
Supply Voltage For Logic	VDD	-0.3	—	4.0	V
Supply Voltage For Panel	Vcc	8	—	19	V
Operating lifetime			20000(*)		Hrs

*:80cd/m^2 light on,50% checkerboard, Frame rate=105HZ, VCC=12V, 25℃ ,50%RH, continued light ON ！

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions ·

Calculation of life from the beginning of product shipments, and customer's storage environment must comply with environmental regulations follows section 12.1 ； and guests are advised to inventory a period not exceeding three months ·

3. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{CI}	—	3.0	3.2	3.3	V
Supply Voltage For Panel	V_{CC}	—	11.5	12	12.5	V
Input High Volt.	V_{IH}	—	$0.8V_{CI}$	—	V_{CI}	V
Input Low Volt.	V_{IL}	—	0	—	$0.2V_{CI}$	V
Output High Volt.	V_{OH}	—	$0.9V_{CI}$	—	V_{CI}	V
Output Low Volt.	V_{OL}	—	0	—	$0.1V_{CI}$	V
*Supply Current(for V_{DD})	I_{DD}	—	—	45	—	mA

*80cd/m^2 light on, Frame rate=105HZ, V_{DD}=3.2V, V_{CC} =12V, 25℃ ,50%RH

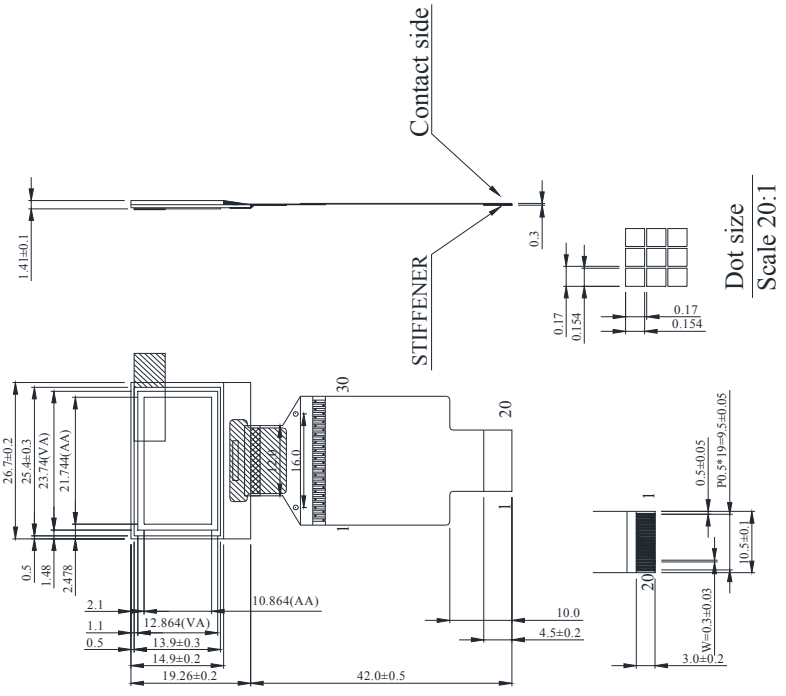
4. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	160	—	—	deg
CIE x(White)	0.25	0.29	0.33	—
CIE y(White)	0.27	0.31	0.35	—
Dark Room contrast	2000:1	—	—	—
Response Time	—	10	—	μs
Brightness w	60	80	100	cd/m^2

5. Dimensional Outlines

PIN NO.	SYMBOL
1	NC(GND)
2	VBAT
3	NC
4	VSS
5	VDD
6	CS#
7	RES#
8	D/C#
9	R/W#
10	E/RD#
11	DB0
12	DB1
13	DB2
14	DB3
15	DB4
16	DB5
17	DB6
18	DB7
19	VCC
20	DISP

The tolerance of non-specified dimension is ±0.2mm.



			UNIT: mm		
			SCALE:		
APPROVE			MODEL L128649A	REV : 0	
CHECK			TITLE LCM DRAWING		
DRAW	*Jame*	*2012/12/05*	DWG NO.		

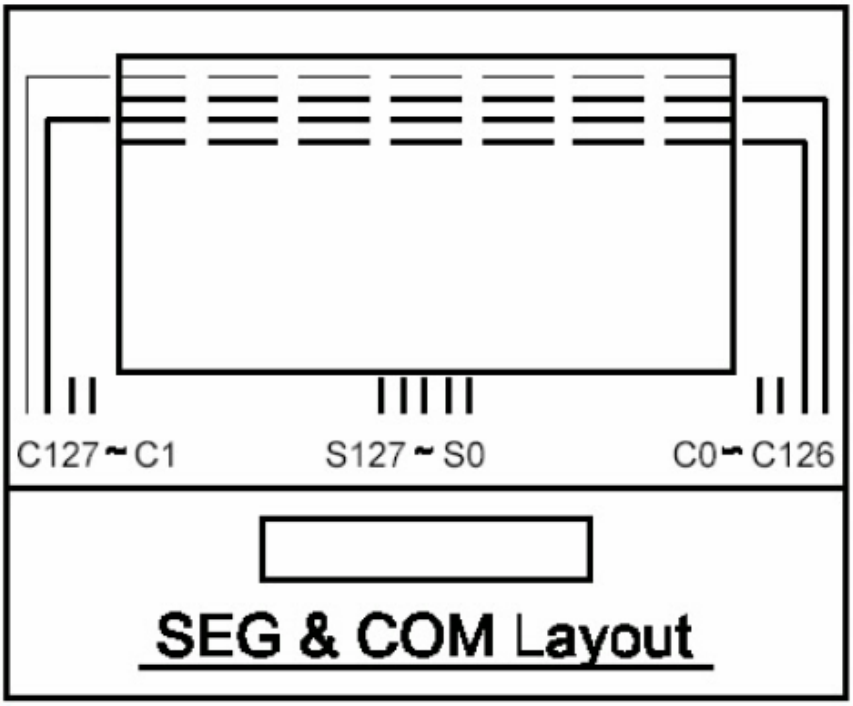
SPECIFICATIONS

STORAGE TEMP : -40°C TO +85°C
OPERATING TEMP : -40°C TO +70°C
VIEWING DIRECTION : ALL
DRIVE CONDITION : 1/64 DUTY
Dot Matrix:128*64
INPUT VOLTAGE(Module):3.0V(TYP)
68XX 8BIT

6. Interface Description

Pin No.	Symbol	Description
1	Vss	Ground
2	VBAT	Power supply for charge pump circuit.(Please NC)
3	NC	NC
4	Vss	Ground
5	V_{DD}	Power supply for logic circuit.
6	CS#	Chip select input.
7	RES#	Reset signal input.
8	D/C	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.
9	R/W	Read/Write select pin.
10	E	Read/Write enable pin
11	DB0	Data bus(for parallel interface)
12	DB1	
13	DB2	
14	DB3	
15	DB4	
16	DB5	
17	DB6	
18	DB7	
19	NC	NC
25	Vss	Ground.

7. Panel Layout Diagram



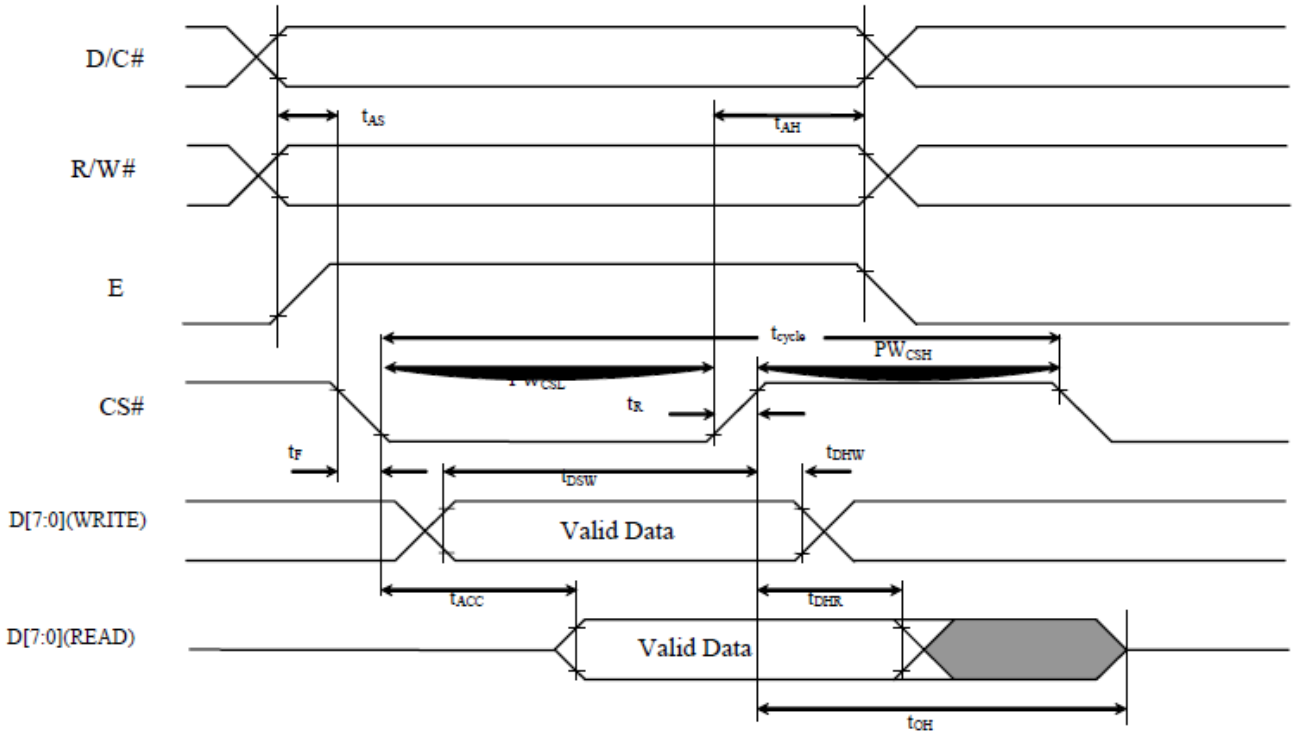
8. Application circuit

Non

9. Timing Characteristics

6800 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

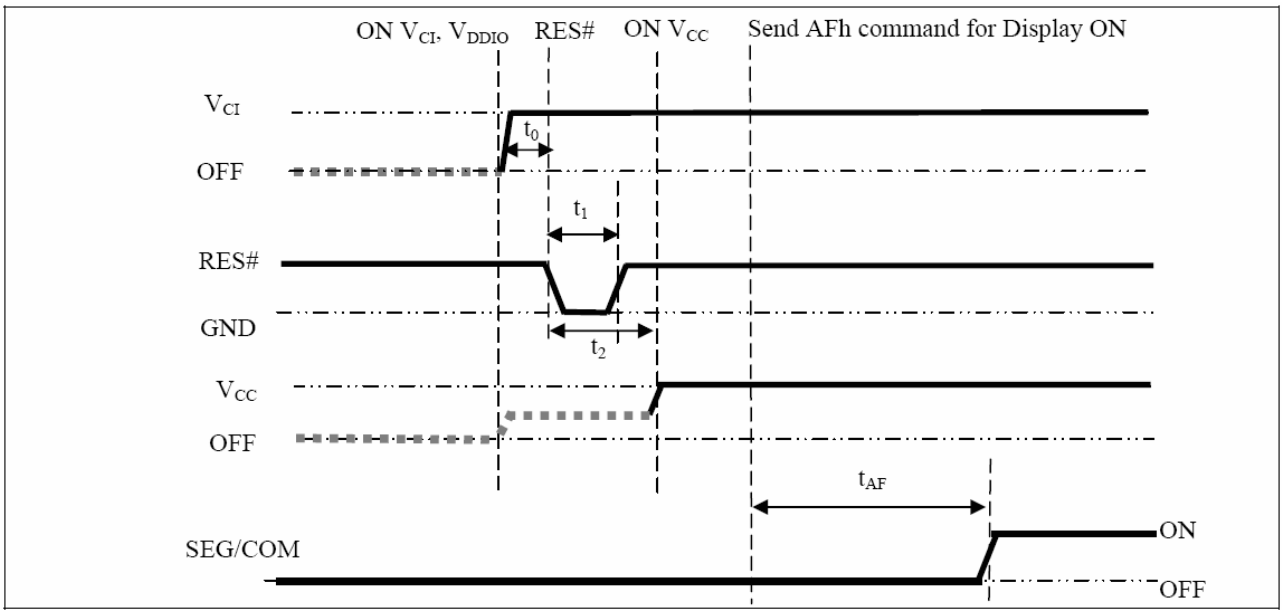


10. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

10.1 POWER ON / OFF SEQUENCE

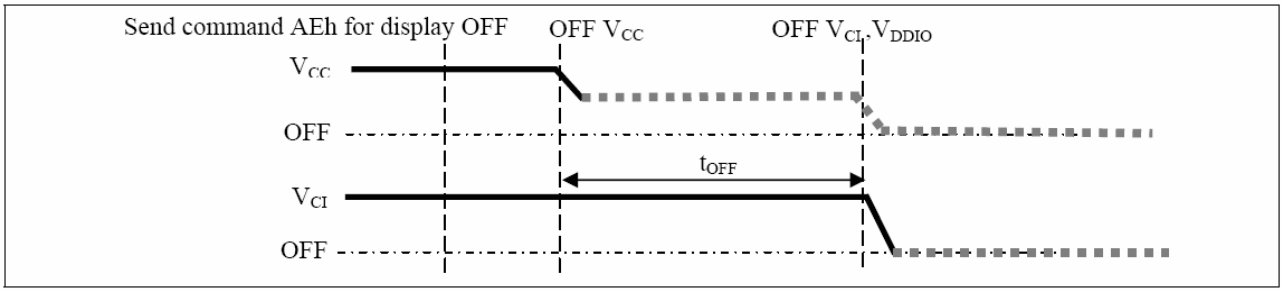
***Power ON sequence**:*

1. Power ON V_{CI}.
2. After V_{CI} becomes stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.(1), (2), (3)
3. Wait for t_{OFF}. Power OFF V_{CI}. (where Minimum t_{OFF}=0ms (5), Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between V_{CI} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be kept float (disable) when it is OFF.

(3) Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.

(4) The register values are reset after t_1.

(5) V_{CI} should not be Power OFF before V_{CC} Power OFF.

11. Display Control Instruction

Command Table

(R/W#(WR#) = 0, E(RD#) = 1 unless specific setting is stated)

1. Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode

2. Scrolling Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	26/27	0	0	1	0	0	1	1	X_0	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 5 frames | 100b – 3 frames 001b – 64 frames | 101b – 4 frames 010b – 128 frames | 110b – 25 frame 011b – 256 frames | 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 The value of D[2:0] must be larger or equal to B[2:0] E[7:0] : Dummy byte (Set as 00h) F[7:0] : Dummy byte (Set as FFh)
0	A[7:0]	0	0	0	0	0	0	0	0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[7:0]	0	0	0	0	0	0	0	0		
0	F[7:0]	1	1	1	1	1	1	1	1		

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	29/2A	0	0	1	0	1	0	X_1	X_0	Continuous Vertical and Horizontal Scroll Setup	29h, X_1X_0=01b : Vertical and Right Horizontal Scroll 2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 | C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 5 frames | 100b – 3 frames 001b – 64 frames | 101b – 4 frames 010b – 128 frames | 110b – 25 frame 011b – 256 frames | 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 | The value of D[2:0] must be larger or equal to B[2:0] E[5:0] : Vertical scrolling offset e.g. E[5:0]= 01h refer to offset =1 row E[5:0] =3Fh refer to offset =63 rows **Note** (1) No continuous vertical scrolling is available.
0	A[2:0]	0	0	0	0	0	0	0	0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh. For example, if "26h; 2Ah; 2Fh." commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A3	1	0	1	0	0	0	1	1	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64] **Note** (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line ($X_5X_4X_3X_2X_1X_0$ of 40h~7Fh) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0]= 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		

3. Addressing Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0	20	0	0	1	0	0	0	0	0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0	A[1:0]	*	*	*	*	*	*	A_1	A_0		
0	21	0	0	1	0	0	0	0	1	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d) B[6:0]: Column end address, range : 0-127d, (RESET =127d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		

3. Addressing Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0]. **Note** (1) This command is only for page addressing mode

4. Hardware Configuration (Panel resolution & layout related) Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~63d The value is reset to 00h after RESET.
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration A[5]=0b(RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap

5. Timing & Driving Scheme Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	D5	1	1	0	1	0	1	0	1	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b Frequency increases as setting value increases.
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	D9	1	1	0	1	1	0	0	1	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	DB	1	1	0	1	1	0	1	1	Set V_{COMH} Deselect Level	
0	A[6:4]	0	A_6	A_5	A_4	0	0	0	0		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation

A[6:4]	Hex code	V_{COMH} deselect level
000b	00h	~ 0.65 x V_{CC}
010b	20h	~ 0.77 x V_{CC} (RESET)
011b	30h	~ 0.83 x V_{CC}

Note
(1) "*" stands for "Don't care".

12. Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	——
2	High temp. (Operation)	70°C, 120hrs	——
3	Low temp. (Operation)	-40°C, 120hrs	——
4	High temp. / High. humidity (Operation)	60°C, 90%RH, 120hrs	——
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	——
6	Vibration	Total fixed amplitude : 1.5mm Vibration Frequency :10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	——
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	——

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

*12.1 Storage Environment Required

Temperature:	23 ± 5°C
Humidity:	10 ± 5% RH

13. Numbering system

V L 12864 9A - W P

① ② ③ ④ ⑤ ⑥ ⑦

1. Brand Name

V	Vitek Display co., LTD

2. Display Type

L	OLED Type

3. Number of Pixels

Graphic Module	Row Dots × Column Dots

4. Series number

1-9	Series Number

5. LCD Mode:

B	Blue
G	Green
W	White
Y	Yellow
C	Color

6. DC/DC

X	Without Positive Voltage
P	Positive Voltage

7. Special code
